A Full Soft Switched Bridgeless Power Factor Corrected AC-DC Converter

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***Abstract*-In this study, a soft swithed and bridgeless power factor corrected (BPFC-FSS) boost converter with an active snubber cell is presented. The converter is operated with pulse with modulation (PWM) and the average current mode control is used to generate PWM signals. The soft switching operation of all semiconductors is achieved by a snubber circuit in introduced converter. The snubber circuit allows zero voltage transition (ZVT) turn on and zero voltage switching (ZVS) turn off for the boost switch. In addition, zero current switching (ZCS) turn on and ZVS turn off of the snubber switch are provided. The boost diode and the other snubber diodes work with soft switching. Moreover, the current stress of the snubber switch is descended by the soft switching energy delivery to the output. Thes soft switching operation of all semiconductors is accomplished for different load case. Thus, the conduction and switching losses are reduced and the efficiency is increased. The theoretical analysis of the BPFC-FSS is presented and validated with a simulation work operating at 100 kHz, with 1 kW output power and 400 V output voltage.**

I. INTRODUCTION

In recent years, the nonlinear electric appliances which create harmonic currents cause decrease of power quality of the system. Therefore, power factor correction (PFC) circuits have become important to improve the power factor of system. A variety of circuit topologies have been developed for PFC applications. The PFC topologies can be employed in switching mode power supplies (SMPS), battery chargers, electronic ballasts and the other industrial applications fed from AC line.

Boost converters have been used widely in different industrial areas, due to high power density, fast transition response, the simple structure and easy to implement. The boost converter following a diode bridge rectifier is the most commonly used in the PFC applications. In conventional boost PFC converter, the current flows through three semiconductor devices, two diodes are at the rectifier stage and one is at the boost stage. These diodes exhibit a forward voltage that leads to conduction losses. Therefore, researchers start to develop new alternatives known as bridgeless PFC to reduce conduction losses. In the BPFC converter, current flows through only two semiconductor devices. Unlike the traditional boost PFC converter, BPFC converter improves efficiency by removing two rectifier diodes.

PFC converters can operate in discontinuous conduction mode (DCM), boundary conduction mode (BCM), and continuous conduction mode (CCM). The CCM operation of the boost converter is generally preferred at high power levels. However, reverse recovery power loss of boost diode leads to reduced efficiency and this power loss worsens when the switching frequency is increased. Electromagnetic interference (EMI) is the important issue at high frequency applications as well. Therefore, soft switching (SS) techniques should be used to overcome problems mentioned above [1]-[4].

In [1], the conventional zero voltage transition (ZVT) PWM converter is proposed. The ZVT turn-on for the boost switch and zero current switching (ZCS) turn off for the boost diode are accomplished very well. However, the snubber switch hardy turn off and it has high current stress. To overcome these problems, different methods have been reported [5]- [18]. In [5], [9] and [15], the boost switch has an extra current stress and the boost diode has extra voltage stress in [6]. The snubber diode has an extra voltage stress in [5], [9]. In [16], extra voltage stress is occurred across the snubber switch. In [11], soft switched turn on process of the main switch worsens at partial load conditions. In [14], the bridgeless SEPIC converter with positive output voltage is introduced. The converter has one switch but three semiconductor components are in power flow path. The main switch works with hard switching condition as well. In [17], [18], The ZVT and zero current transition (ZCT) techniques are adopted for bridgeless PFC converter. Thanks to auxiliary circuit, there are no extra voltage and current stress on the main switches.

In the soft switching techniques addressed above, the current stress of the snubber switch is high because of the discharge of the capacitor parallel connected to the boost switch. The soft switching techniques presented in [16], [19]-[22], reduce current stress of the snubber switch in the boost converter. In these studies, soft switched turn on for the boost switch is accomplished and low current stress of the snubber switch as well. The low current stress is accomplished by a transformer used in a snubber circuit. The presented snubber circuit in [16] and [21], works a transformer and this transformer requires high magnetizing inductance. Besides, the energy of the magnetizing inductance is absorbed by passive components. This magnetizing energy results in extra voltage stress across the snubber switch as well. The introduced snubber cell in [20] needs a center tapped transformer to provide low current stress across the snubber

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switch. The snubber switch operates with soft switching as well. However, SS turn off for the snubber switch deteriorates at light load conditions.

In this study, a bridgeless power factor corrected full soft switched (BPFC-FSS) converter which overcomes many of problems discussed before is constructed. In the converter, the boost switch work with soft switching; it turns on with ZVT and turns off with almost ZVS. The snubber switch turns on with almost ZCS and turns off with almost ZVS. All diodes including boost and the other snubber diodes work with soft switching and they have no an extra voltage stress. The boost switch and diode have no extra current stress. In the snubber cell of the BPFC-FSS converter, since the most of the SS energy is delivered to the output, the current stress of the snubber switch is reduced. In addition, the BPFC architecture reduces the conduction losses and used SS technique work well for different load cases. The operation modes of the BPFC-FSS converter is analyzed in detail, and simulation results are given at 100 kHz with 1 kW output power and 400 V output voltage.

II. Operation Principles of The Proposed Converter

The circuit diagram of the proposed BPFC-FSS converter in Fig. 1 consist of two parts; the boost and the snubber circuits. In the boost circuit, v_{ac} is the input voltage and rectified from the input voltage, i_{ac} is input current, V_o is the output voltage, L_B is the boost inductor, T_{B1} and T_{B2} are the boost switches, driven with same PWM signals, D_{B1} and D_{B2} are the boost diodes, D_{TB1} and D_{TB2} are the body diodes of the boost switch. In the snubber circuit, T_S is snubber switch, L_{S1} and L_{S2} are the snubber inductors, C_{S1}, C_{S2} and C_{S3} are the snubber capacitors and D_{S1}-D_{S5} are used as the snubber diodes.

In a half line cycle, the boost inductor of the BPFC-FSS is energized with the conduction of T_{B1} and D_{TB2} then stored energy in the boost inductor is transferred to the output by D_{B1}. In the second half line cycle, another boost operation is occurred by the conduction of T_{B2}, D_{TB1} and D_{B2}.

In the analysis of the BPFC-FSS, the operation of the first half line cycle is took into consideration. All of used semiconductor components are assumed as ideal except D_{B1}, D_{B2}. The current of L_B inductance and the voltage of C_o are accepted as constant in one switching cycle. Based on these assumptions, the converter operation in a switching cycle can be divided into eleven operations. The waveforms for the operation of the BPFC-FSS converter is illustrated in Fig. 2.

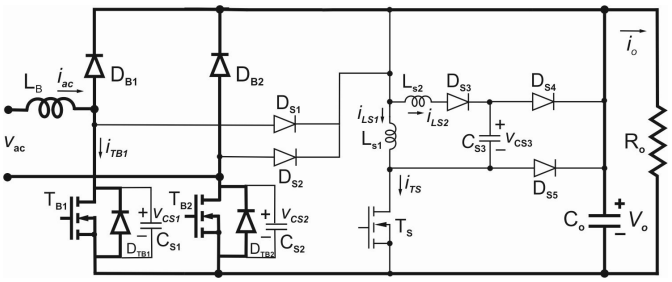

Fig. 1 The circuit scheme of the proposed BPFC-FSS converter.

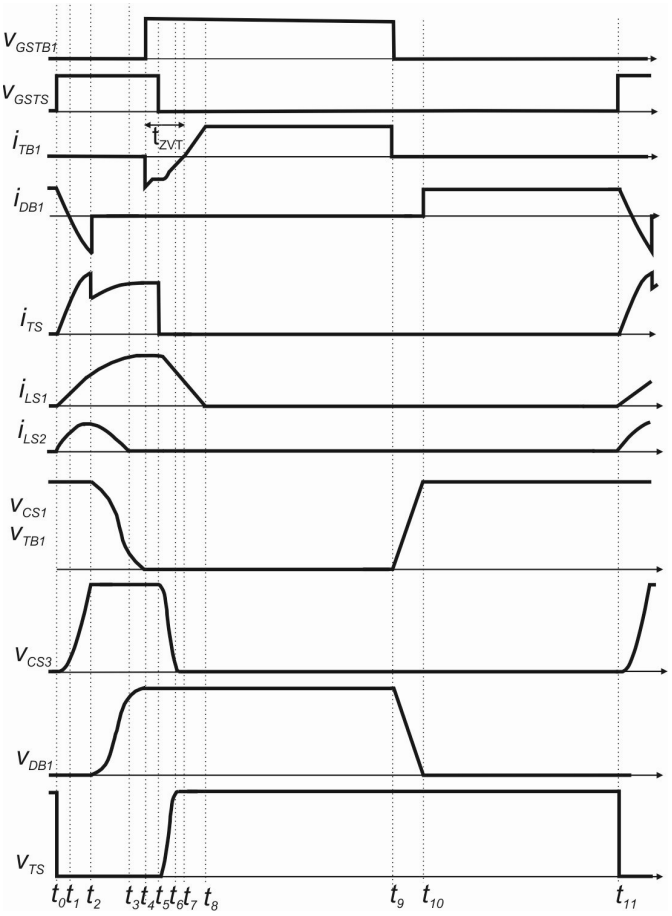

Fig. 2 The waveforms of proposed BPFC-FSS converter.

At $t=t_o$, it is assumed that the input current flows through the D_{B1} diode. When the PWM signal is applied to T_S, it turns on with almost ZCS and i_{LS2} current increases with the resonance occurred between L_{S2} and C_{S3}. At the same time, C_{S3} capacitor charges and the current of L_{S1} increases. The equation for this mode can be defined as follows:

$$L_{S1}\frac{di_{L1}}{dt} = V_o \tag{1}$$

$$L_{S2}\frac{di_{LS2}}{dt} = V_o - v_{CS3} \tag{2}$$

$$C_{S3}\frac{dv_{S3}}{dt} = I_i - i_{LS1} \tag{3}$$

At $t=t_1$, i_{DB1} drop to zero and the i_{LS1} reaches to the input current. The reverse recovery current begins to flow in D_{B1}.

At $t=t_2$, v_{CS3} equals to V_o, D_{S4} turns on with ZVS and D_{B1} turns off with ZCS. When the boost diode turns off, another resonance starts between L_{S1}, L_{S2} and C_{S1}. In this resonant mode, C_{S1} capacitor discharges, L_{S1} current increases and L_{S2} current decreases. At the same time, D_{S4} is still on state and the current of L_{S2} is delivered to the output. The equations of this operation can be extracted as below:

$$L_{S1}\frac{di_{LS1}}{dt}+L_{S2}\frac{di_{LS2}}{dt}=V_o \tag{4}$$

$$C_{S1}\frac{dv_{CS1}}{dt}=i_{LS1} \tag{5}$$

$$i_{TS}=i_{LS1} \tag{6}$$

At $t=t_3$, the current flowing through L_{S2} current descends to zero, D_{S4} is turned off. Another resonance occurs between L_{S1} and C_{S1}. This resonance maintains the decrease of the voltage of C_{S1} and the increase of the current of L_{S1}. The equations representing the behavior of the operation can be given as follow:

$$L_{S1}\frac{di_{LS1}}{dt}=v_{CS1} \tag{7}$$

$$C_{S1}\frac{dv_{CS1}}{dt}=i_{LS1}. \tag{8}$$

Then, C_{S1}'s voltage drops to zero and the body diode of the T_{B1} begins to carry the current. Thus, during the conduction of D_{TB1}, T_{B1} switch can be turned on with ZVT. At time $t=t_4$, C_{S1} voltage drops to zero.

At $t=t_5$, the snubber switch turns off and the current of L_{S1} discharges the C_{S3} capacitor by the conduction of D_{S4}. Because of the resonance happened between L_{S1} and C_{S3}, T_S turns off with almost ZVS.

At $t=t_6$, when the voltage of C_{S3} capacitor drops to zero and the snubber switch turns off, D_{S5} diode is turned on with ZVS.

At $t=t_7$, when the current of L_{S1} drops to input current I_i, T_{B1} switch turns on with ZVT.

At $t=t_8$, D_{S5} diode turns off when the current of L_{S1} drops to zero and the current of T_B reaches I_i. As a result, the on stage of traditional boost converter starts to work.

At $t=t_9$. T_{B1} and T_{B2} are turned off with ZVS. The current of L_B charges the C_{S1} capacitor by turn off of T_{B1} and T_{B2}.

At $t=t_{10}$, D_{B1} diode turns on under the ZVS condition when C_{S1} capacitor charges to V_o.

At $t=t_{11}$, the one switching cycle is completed.

III. DESIGN PROCEDURE

A. SNUBBER CIRCUIT DESIGN

To achieve soft switching conditions of the snubber switch and the boost diodes, following equations can be used.

$$L_{S1}\geq\frac{V_o}{I_i}t_{rTs} \tag{9}$$

$$L_{S1}\geq\frac{V_o}{I_i}3t_{rr}. \tag{10}$$

Here, t_{rTs} is the rising time of T_S and t_{rr} is the reverse recovery time of D_{B1}. The ZCS turn on for snubber switch and turn off for boost diode is provided by the snubber inductance.

To achieve ZVS turn off for T_{B1} and T_{B2} switch, the voltage of switches must reach V_o in the falling time, t_{fTB}. Thus, C_{S1} and C_{S2} can be calculated as follows:

$$C_{S1}\geq\frac{I_i}{V_o}t_{fTB1} \tag{11}$$

$$C_{S2}\geq\frac{I_i}{V_o}t_{fTB2}. \tag{12}$$

Above, t_{fTB1} and t_{fTB2} represent the falling time of T_{B1} and T_{B2}.

The snubber capacitor C_{S3} provides the ZVS turn off for the snubber switch, it can be calculated as follows:

$$C_{S3}\geq\frac{I_i}{V_o}t_{fTs} \tag{13}$$

Here, t_{fTs} is the falling time of the snubber switch.

B. CONTROL CIRCUIT DESIGN

In the control method of BPFC-SS converter, average current mode control is used to generate PWM signals both boost and snubber switch. T_{B1} and T_{B2} can be driven with same signal. The PWM signal of T_s should be applied just before the control signal of T_{B1} or T_{B2} and ends after turn on of T_{B1} or T_{B2}. It is also assumed that the converter is operated with CCM which means that the current of L_B never falls to zero.

The average current mode control used to obtain sinusoidal input current for the proposed BPFC-SS converter, consists of two parts which are the current control loop design and the voltage control loop design. The block diagram of average current mode control is shown in Fig. 3.

In the voltage control loop design, the sensed output voltage $v_{o\text{-}sensed}$ is compared to the reference output voltage v_{ref} and an error is produced. This error is multiplied with sensed sinusoidal reference current obtained from the rectified line voltage $v_{i\text{-}sensed}$. Thus, a reference signal i_{ref} is obtained then compared to the measured inductor current $i_{LB\text{-}sensed}$. The boost switches T_{B1} and T_{B2} are switched according to produced error to provide high power factor.

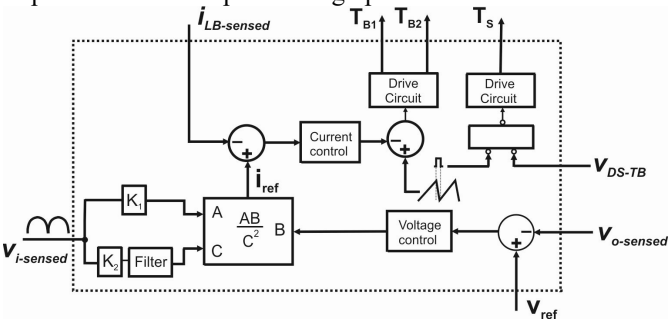

Fig. 3 The block diagram of average current mode control.

C. POWER CIRCUIT DESIGN

In the power stage design, L_B inductor is determined to

provide PFC and operate in CCM. Thus, L_B can be defined based on following equation for universal line voltage range.

$$L_B = \frac{V_{ac(min)}.D}{f_s.\Delta I} \quad (14)$$

Above, ΔI represents the inductor ripple current flowing in L_B and D is the maximum duty ratio at low line voltage $V_{ac(min)}$. The acceptable ripple current can be selected as 20% to provide PFC.

The current stress of power semicondcutors can be defined based on the peak line current. The peak line current, $I_{ac(pk)}$, can be defined as follows at low line

$$I_{ac(pk)} = \frac{2.P_o}{\sqrt{2}.V_{ac(min)}}. \quad (15)$$

The filter capacitor C_o is determined took into consideration of the output voltage ripple, output power and hold-up time requirement.

The voltage stress of power semiconductors are limited by the output voltage.

IV. Simulation Results

A simulation study is performed to validate the proposed operation of the BPFC-SS converter. The simulation work is operated for 400 V output voltage and 1 kW output power. The switching frequency is selected as 100 kHz and 220 V_{ac} input voltage is applied to the converter. PSIM program is used to validate the operation of BPFC-SS converter. The simulated circuit schematic of proposed converter is shown in Fig. 4.

According to design procedure given in previous section, the circuit parameters are determined as, L_B=200 µH, C_o=960µF, L_{S1}=12 µH, L_{S2}=6 µH, C_{S1}, C_{S2}=2 µF, C_{S3}=1 µF. The power semiconductors are selected according to their voltage and current stress defined in previous section. The used components and their performance are summarized in Table I.

TABLE I. The Power Semiconductors Used in the Simulation of BPFC-SS Converter.

Semiconductors	Part Name / Specifications
T_{B1}, T_{B2}	IXFK36N60 / 600 V – 36 A
D_{B1}, D_{B2}	DSEI19-06AS / 600 V – 20 A
T_S	IXFH20N60Q / 600 V – 20 A
D_{S1}-D_{S4}	DSEI19-06AS / 600 V – 20 A

The implemented control signals for the boost and snubber switches are shown in Fig. 5.

The boost switch turns on with ZVT and turns off with ZCS as shown in Fig. 6. ZVT turn on is achieved with the conduction of D_{TB1}. At the turn off process, ZVS turn off of T_B is achieved by the C_{S2}'s charge. The voltage stress of the switch is reduced.

The soft switching operation of the snubber switch is given in Fig. 7. The snubber switch turns on with ZCS and turns off with ZVS. The reduced current stress of the snubber switch achieved and additional voltage stress across the snubber switch is not occurred.

The waveforms for the boost diode is given in Fig. 8. The voltage stress of the diode is restricted by the output voltage. It turns on with ZVS and turns off with ZCS.

As it can be seen in Fig 9, the waveforms of the input voltage and the current are almost in same phase. The power factor (PF) is obtained as 0.998, very close to unity, at full power and total harmonic distortion of the line current (THD_i) is obtained as %4, at full power. Fig. 10 gives the input voltage and current waveform at with PF measurement, at 50% load condition. The PF is measured as 0.989 at half power. The PSIM simulation have function providing PF and THDi measurement. The obtained PF and THD values are extracted directly from transient analysis in the simulation. In the simulation work, the efficiency of the BPFC-FSS is measured as %97.4 at full load condition.

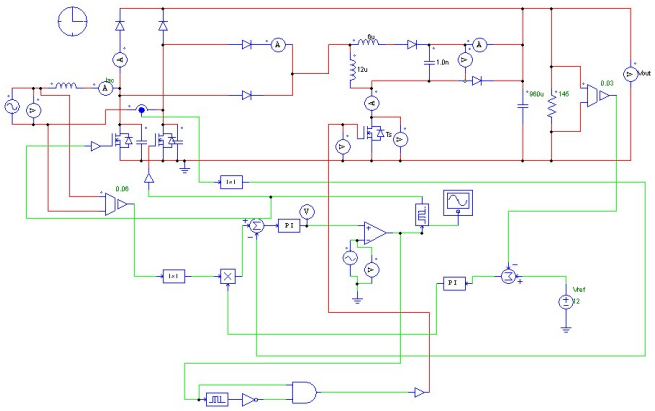

Fig. 4 The simulation schematic of the proposed BPFC-FSS converter.

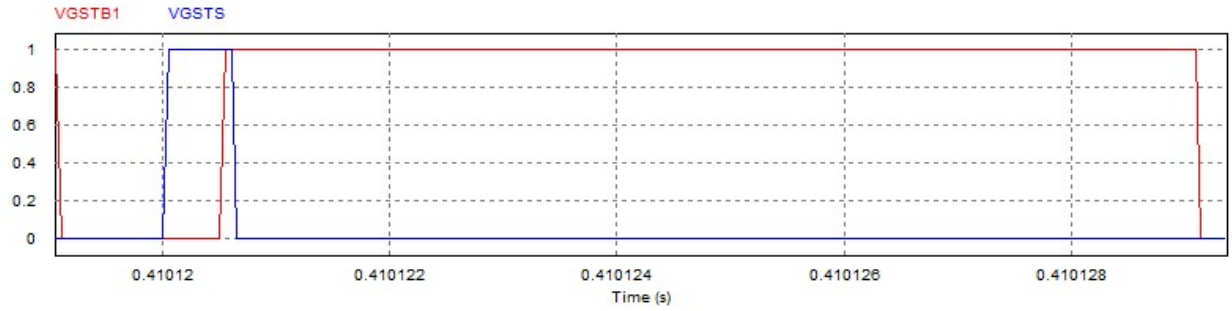

Fig. 5. The control signals of the boost switch, $V_{GS\text{-}TB1}$, and the snubber switch, $V_{GS\text{-}TS}$.

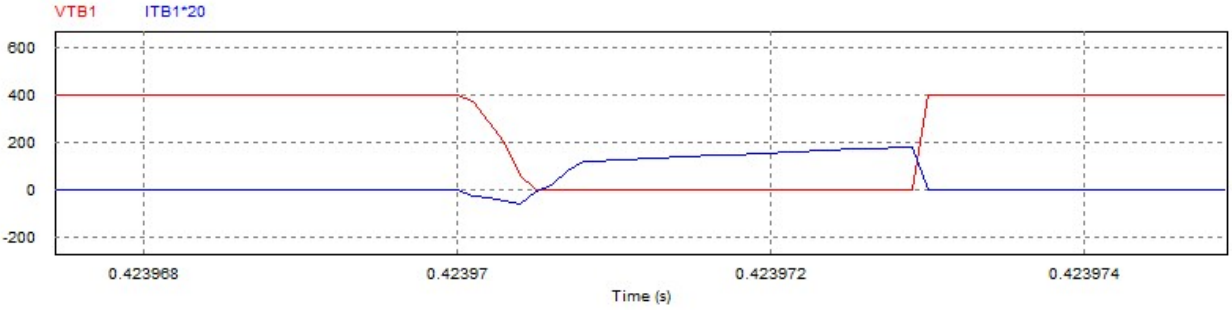

Fig. 6 The current and voltage waveforms of the boost switch, i_{TB1} and v_{TB1}.

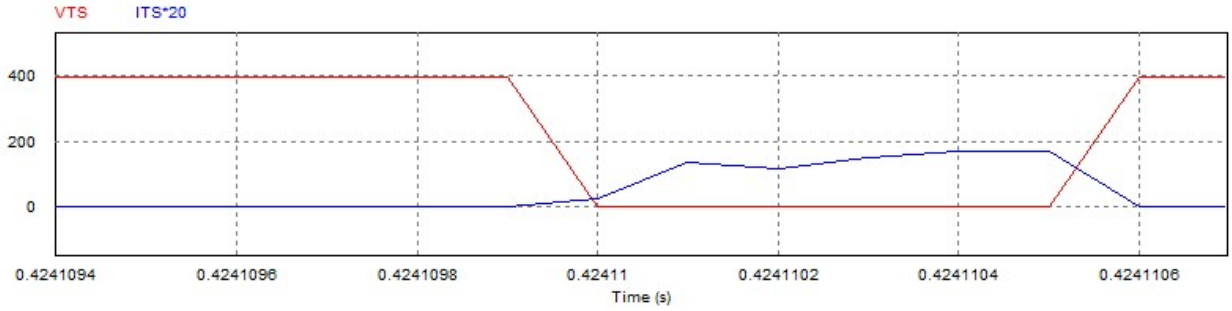

Fig. 7 The current and voltage waveforms of the snubber switch, i_{TS} and v_{TS}.

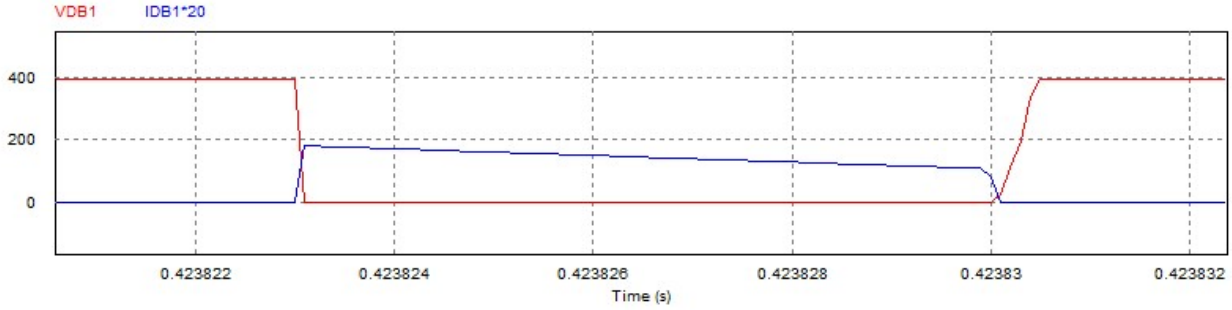

Fig. 8 The current and the voltage waveforms of the boost diode, i_{DB1} and v_{DB1}.

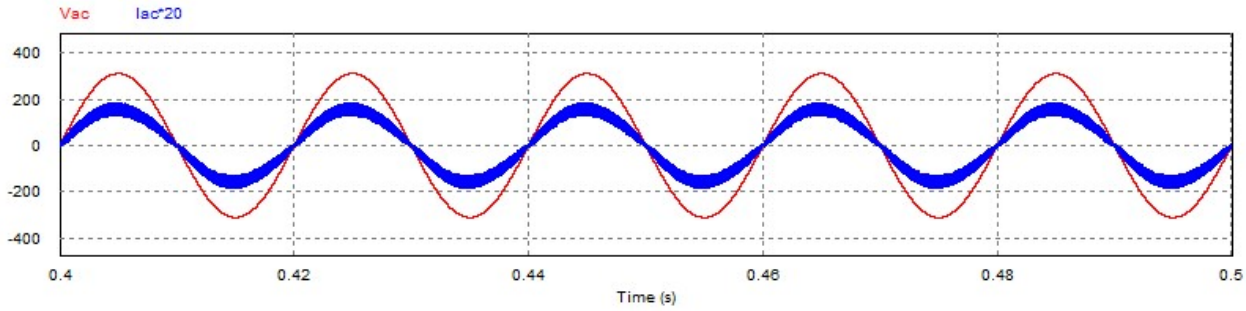

Fig. 9 The line voltage (v_{ac}) and input line current (i_{ac}) waveforms of the BPFC-SS converter at full power.

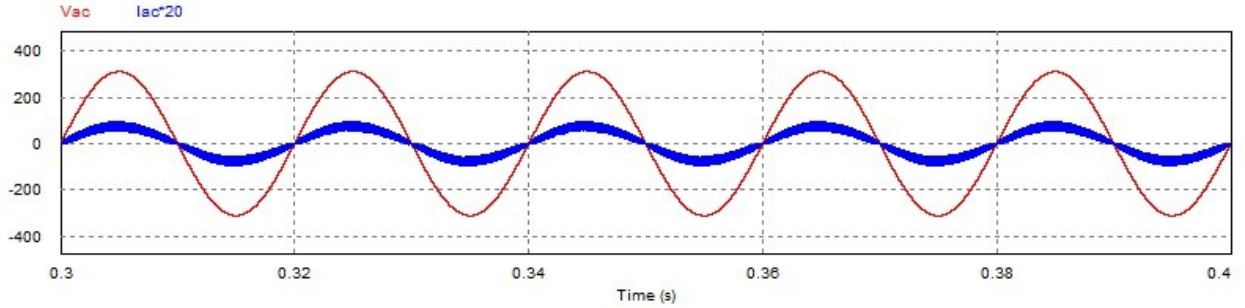

Fig. 10 The line voltage (v_{ac}) and input line current (i_{ac}) waveforms of the BPFC-SS converter at 50% load.

V. CONCLUSIONS

In this work, a full soft switched bridgeless power factor corrected AC-DC converter is presented. In the presented converter, all semiconductor devices are soft switched and their voltage stress are suppressed by the output voltage. The presented snubber circuit accomplishes low current stress for the snubber switch by the transfer of soft switching energy to the output. In order to verify the system performance, the converter performed by a simulation study which operates with 1 kW output power and 400 V output voltage, at 100 kHz operation frequency. The simulation results give coherent results compared to the presented theoretical analysis.

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