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Single DDCC− based simulated floating inductors and their applications

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Ahmet Abaci[1], *Erkan Yuce*[1] ✉

[1]*Department of Electrical and Electronics Engineering, Pamukkale University, 20160 Kinikli, Denizli, Turkey*
✉ *E-mail: erkanyuce@yahoo.com*

Abstract: Three simulated floating inductor (SFI) circuits containing a single DDCC− called as minus-type differential difference current conveyor are proposed. These SFIs are series lossy, parallel lossy and negative lossless ones. The used DDCC− in each of the proposed SFIs has a single Z terminal. Without needing any passive element matching constraints, each of the proposed SFIs is composed of a minimum number of passive elements. As application examples, second-order current-mode (CM) and voltage-mode low-pass (LP) filters derived from the proposed series lossy SFI are given. Also, a fourth-order CM Butterworth LP filter example is presented as another application. A second-order CM high-pass (HP) filter and an RLC resonant circuit obtained from the proposed parallel lossy SFI are given. All the simulations are achieved via SPICE program. Moreover, some experimental results for the proposed lossy SFIs and CM HP filter are given in order to show the performances.

1 Introduction

The employment of current-mode (CM) active building blocks (ABBs) called as differential difference current conveyors (DDCCs), second-generation current conveyors (CCIIs), current feedback operational amplifiers (CFOAs) and so on possess some potential advantages in contrast to operational amplifiers [1–3]. These advantages are wide bandwidth, great dynamic range, good linearity, usage of a smaller number of elements and so on. The DDCC combines the advantages of both the CCII and differential difference amplifier that has the capability of arithmetic operations. Moreover, the DDCC finds wide application areas as declared in [4]. DVCC called as differential voltage current conveyor can be easily realised from the DDCC. DVCC/DDCC based on a number of simulated inductors (SIs) [5–18] have been reported in the literature. DVCC/DDCC based SIs can be divided into two subcategories such as simulated grounded inductors (SGIs) [5–8, 16, 18] and simulated floating inductors (SFIs) [9–18]. Nonetheless, SFIs developed in [9–18] possess the following disadvantages: some of them employ more than one DVCC/DDCC [9–15]. Several SFIs suffer from a matching condition [10, 16, 17]. Some of SFIs use DVCC/DDCC with more than one Z terminal [9–12, 14–18]; thus, they have limited high frequency performances due to frequency-dependent non-ideal current gains. In addition to these, CCII based SFIs [19–24], CFOA based SFIs [25–29] and other ABB based SIs [30–38] were published in the literature before. However, the circuits of [34, 36] are SGIs. The circuits of [19–31, 33, 35, 37] include more than one ABB. The circuits of [22, 25, 31] need a matching condition. Some SIs [32–38] contain an operational transconductance amplifier (OTA) in their internal structures; therefore, they have restrictions at high frequencies as mentioned in [39]. Apart from these, DVCC/DDCC based on a number of analogue circuits such as first-order voltage-mode (VM) all-pass filters [40–44], first-order CM all-pass filter [45], shadow filters [46], second-order VM filters [47–50], high-order filter [51], oscillators [52, 53] and so on have been reported in the literature so far.

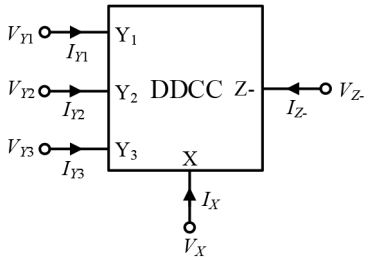

Fig. 1 *Electrical symbol of five-terminal DDCC*

Single minus-type DDCC (DDCC−) based series lossy, parallel lossy and negative lossless SFI circuits are proposed. The used DDCC− in each of the proposed SFIs has a single Z terminal. Without needing any matching constraints, each of the proposed SFIs is composed of a minimum number of passive elements. As applications, second-order CM and VM low-pass (LP) filters, a fourth-order CM Butterworth LP filter example derived from the proposed series lossy SFI are presented. Also, a second-order CM high-pass (HP) filter and an RLC resonant circuit obtained from the proposed parallel lossy SFI are given. In all the AC and transient simulations achieved through SPICE program, 0.13 µm IBM technology parameters given in [50] are utilised. In addition, several experimental results for the proposed lossy SFIs and CM HP filter are given in order to show the performance.

After the introduction, the proposed DDCC based series lossy, parallel lossy and negative lossless SFIs are depicted in Section 2. In Section 3, the presented application examples derived from the proposed SFIs are described. As an example, parasitic impedance effects on the performances of the proposed negative lossless SFI are given in Section 4. In Sections 5 and 6, simulation and experimental results are discussed, respectively. This manuscript is ended in Section 7.

2 Proposed DDCC− based SFIs

Electrical symbol of a five-terminal DDCC− is depicted in Fig. 1. Considering all the non-ideal gains, the DDCC− is defined as

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} \beta_1 & -\beta_2 & \beta_3 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\gamma \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{bmatrix} \quad (1)$$

Here, β_j ($j = 1, 2, 3$) are non-ideal voltage gains and γ is non-ideal current gain, which are all ideally equal to unity. Using a single pole model, non-ideal gains can be defined as

$$\beta_1(f) = \frac{\beta_{1o}}{1 + (jf/f_{\beta 1})} \tag{2a}$$

$$\beta_2(f) = \frac{\beta_{2o}}{1 + (jf/f_{\beta 2})} \tag{2b}$$

$$\beta_3(f) = \frac{\beta_{3o}}{1 + (jf/f_{\beta 3})} \tag{2c}$$

$$\gamma(f) = \frac{\gamma_o}{1 + (jf/f_{\gamma})} \tag{2d}$$

where β_{jo} ($j = 1, 2, 3$) are DC non-ideal voltage gains while γ_o is DC non-ideal current gain. Further, $f_{\beta 1}$, $f_{\beta 2}$, $f_{\beta 3}$ and f_{γ} are related pole frequencies. The proposed series lossy SFI, parallel lossy SFI and negative lossless SFI circuits are shown in Figs. 2–4, respectively.

The proposed series lossy SFI can be represented by

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{sCR_1R_2 + 2R_1} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \frac{1}{sL_{eq} + R_{eq}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{3}$$

Here, $L_{eq} = CR_1R_2$ and $R_{eq} = 2R_1$. From (3), quality factor (Q) [54] is computed as

$$Q = \frac{\omega L_{eq}}{R_{eq}} \tag{4}$$

It is observed from (4) that the proposed series lossy SFI can be operated as a lossless inductor in the following frequency range:

$$Q = \frac{2\pi f CR_2}{2} \geq 10 \Rightarrow f \geq \frac{10}{\pi} \frac{1}{CR_2} \tag{5}$$

The proposed parallel lossy SFI can be represented by

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \left(\frac{1}{sCR_1R_2} + \frac{2}{R_1} \right) \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \left(\frac{1}{sL_{eq}} + \frac{1}{R_{eq}} \right) \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{6}$$

where $L_{eq} = CR_1R_2$ and $R_{eq} = R_1/2$. From (6), Q is computed as

$$Q = \frac{R_{eq}}{\omega L_{eq}} \tag{7}$$

It is seen from (7) that the proposed parallel lossy SFI can be operated as a lossless inductor in the following frequency range:

$$Q = \frac{1}{4\pi f CR_2} \geq 10 \Rightarrow f \leq \frac{1}{40\pi CR_2} \tag{8}$$

The proposed negative lossless SFI can be represented by

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = -\frac{1}{sCR_1R_2} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = -\frac{1}{sL_{eq}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{9}$$

Here, $L_{eq} = CR_1R_2$. Electrical symbols of the proposed series lossy, parallel lossy and negative lossless SFIs are, respectively, depicted in Figs. 5–7.

I_1 of the series lossy SFI in Fig. 2 with non-ideal gains is evaluated as

$$I_1 = \frac{1}{sCR_1R_2 + R_1(1 + \beta_2)} (aV_1 + bV_2) \tag{10}$$

where

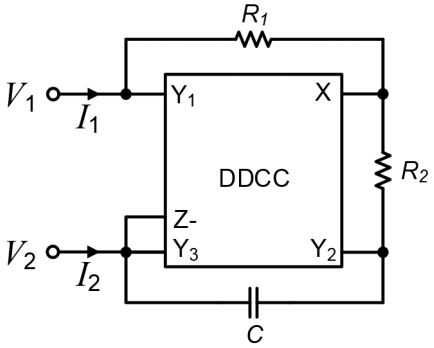

Fig. 2 *Proposed series lossy SFI circuit*

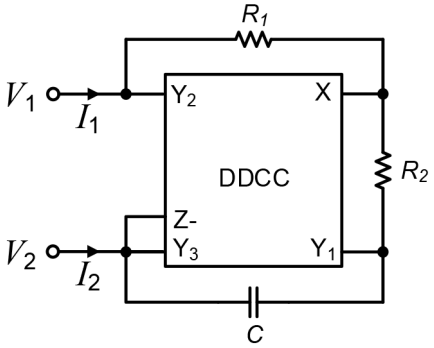

Fig. 3 *Proposed parallel lossy SFI circuit*

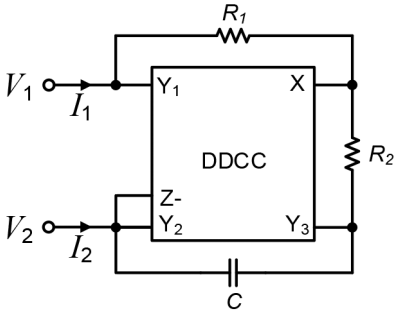

Fig. 4 *Proposed negative lossless SFI circuit*

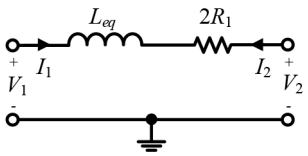

Fig. 5 *Electrical symbol of the series lossy floating inductor*

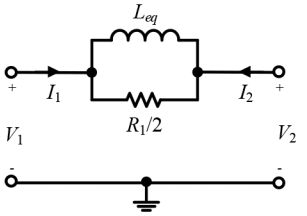

Fig. 6 *Electrical symbol of the parallel lossy floating inductor*

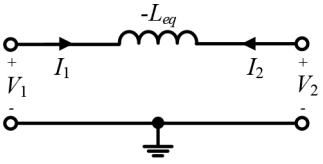

Fig. 7 *Electrical symbol of the negative lossless floating inductor*

$$a = sCR_2(1-\beta_1) + 1 - \beta_1 + \beta_2 \tag{11a}$$

$$b = sCR_2(\beta_2 - \beta_3) - \beta_3 \tag{11b}$$

Similarly, I_2 is evaluated as

$$I_2 = -\frac{1}{sCR_1R_2 + R_1(1+\beta_2)}(cV_1 + dV_2) \tag{12}$$

where

$$c = sCR_1\beta_1(1-\gamma) + sCR_2\gamma(1-\beta_1) + \gamma(1-\beta_1+\beta_2) \tag{13a}$$

$$d = sCR_1(\beta_2 - \beta_3 + 1)(\gamma - 1) + sCR_2\gamma(\beta_2 - \beta_3) - \gamma\beta_3 \tag{13b}$$

I_1 of the parallel lossy SFI given in Fig. 3 with non-ideal gains is calculated as

$$I_1 = \frac{1}{sCR_1R_2 + R_1(1-\beta_1)}(aV_1 + bV_2) \tag{14}$$

where

$$a = sCR_2(1+\beta_2) + 1 - \beta_1 + \beta_2 \tag{15a}$$

$$b = -sCR_2(\beta_1 + \beta_3) - \beta_3 \tag{15b}$$

Likewise, I_2 is calculated as

$$I_2 = -\frac{1}{sCR_1R_2 + R_1(1-\beta_1)}(cV_1 + dV_2) \tag{16}$$

Here

$$c = sCR_1\beta_2(\gamma - 1) + sCR_2\gamma(1+\beta_2) + \gamma(1-\beta_1+\beta_2) \tag{17a}$$

$$d = sCR_1(1-\beta_1-\beta_3)(\gamma - 1) - sCR_2(\beta_1 + \beta_3)\gamma - \beta_3\gamma \tag{17b}$$

I_1 of the negative lossless SFI depicted in Fig. 4 with non-ideal gains is computed as

$$I_1 = -\frac{1}{sCR_1R_2 + R_1(1-\beta_3)}(aV_1 + bV_2) \tag{18}$$

where

$$a = sCR_2(\beta_1 - 1) + \beta_1 + \beta_3 - 1 \tag{19a}$$

$$b = sCR_2(\beta_3 - \beta_2) - \beta_2 \tag{19b}$$

Likewise, I_2 is computed as

$$I_2 = -\frac{1}{sCR_1R_2 + R_1(1-\beta_3)}(cV_1 + dV_2) \tag{20}$$

where

$$c = sCR_1\beta_1(1-\gamma) + sCR_2\gamma(1-\beta_1) + \gamma(1-\beta_1-\beta_3) \tag{21a}$$

$$d = sCR_1(\gamma - 1)(1+\beta_2-\beta_3) + sCR_2(\beta_2 - \beta_3) + \beta_2\gamma \tag{21b}$$

3 Application examples

The presented CM and VM LP filters derived from the proposed series lossy SFI in Fig. 2 are, respectively, depicted in Figs. 8 and 9. Also, a fourth-order CM Butterworth LP filter is presented in Fig. 10. The presented CM and VM filters can provide LP transfer function (TF) as

$$H(s) = \frac{1}{s^2C_1C_2R_1R_2 + 2sC_1R_1 + 1} \tag{22}$$

One can observe from Figs. 8 and 10 that an additional current follower (CF) is required to obtain high output impedance current.

The presented HP filter derived from the proposed parallel lossy SFI is shown in Fig. 11. The presented CM HP filter given in Fig. 11 can provide HP TF as follows:

$$\frac{I_{HP}}{I_{in}} = \frac{s^2C_1C_2R_1R_2}{s^2C_1C_2R_1R_2 + 2sC_2R_2 + 1} \tag{23}$$

Similarly, one can observe from Fig. 11 that an extra CF is needed to obtain high output impedance current. As another application of the parallel lossy SFI is RLC resonant circuit that is denoted in Fig. 12.

Routine analysis of the RLC resonant circuit in Fig. 12 yields the following matrix equation:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \left(\frac{2sC_2R_2 + 1}{sC_2R_1R_2} + sC_1\right)\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{24}$$

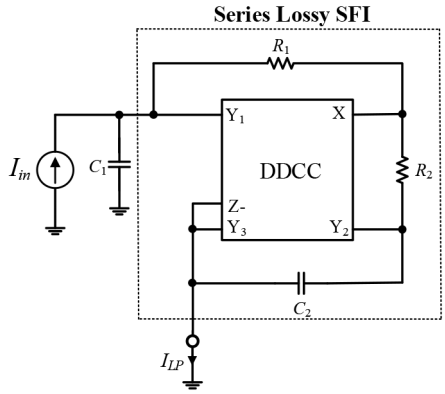

Fig. 8 *Presented CM LP filter*

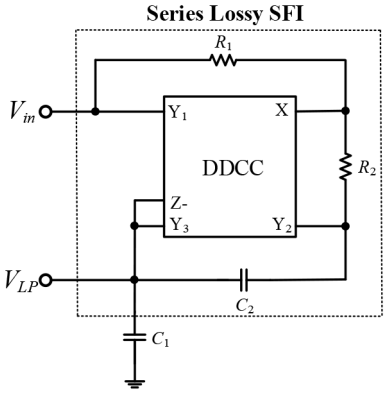

Fig. 9 *Presented VM LP filter*

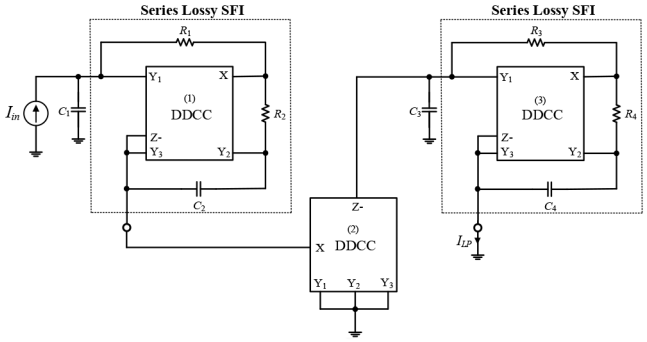

Fig. 10 *Presented fourth-order CM Butterworth LP filter*

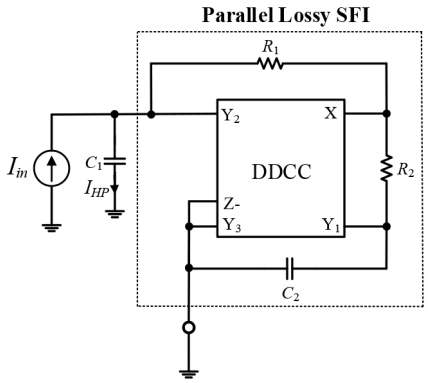

Fig. 11 *Presented CM HP filter*

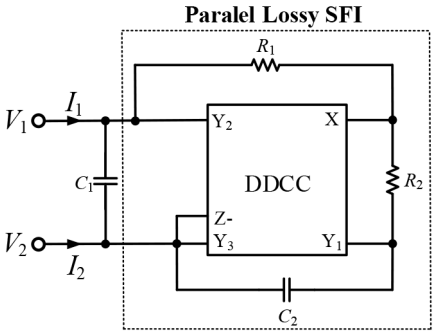

Fig. 12 *Presented RLC resonant circuit*

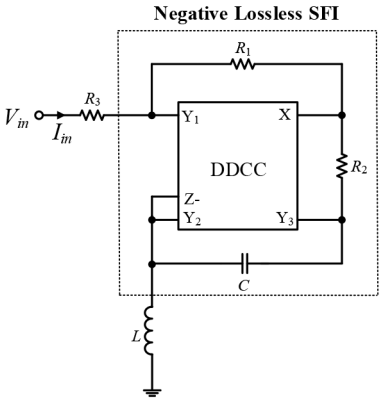

Fig. 13 *Application of the proposed negative lossless SFI*

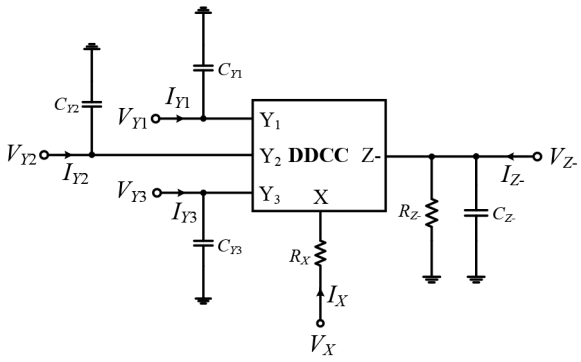

Fig. 14 *DDCC− with its X, Z- Y_1, Y_2 and Y_3 terminal parasitic impedances*

An application example for the proposed negative lossless SFI is given in Fig. 13 where the effects of a parasitic inductor are reduced or cancelled.

It is seen from Fig. 13 that input current, I_{in} is found as

$$I_{\text{in}} = \frac{V_{\text{in}}}{R_3} \tag{25}$$

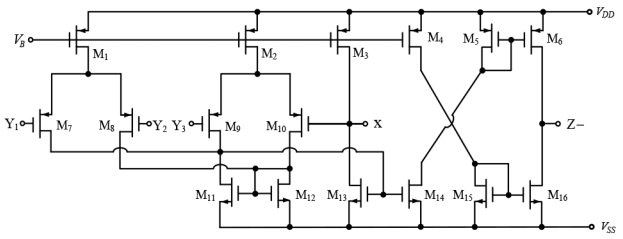

Fig. 15 *MOS transistor based DDCC− derived from [4]*

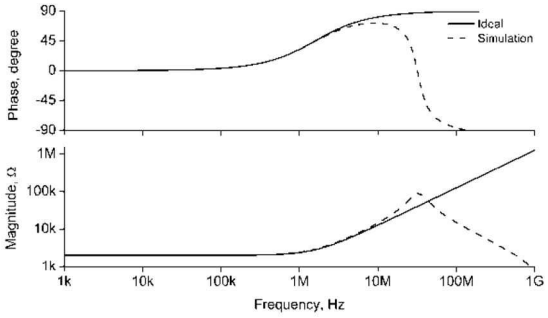

Fig. 16 *AC analysis for the proposed series lossy SFI*

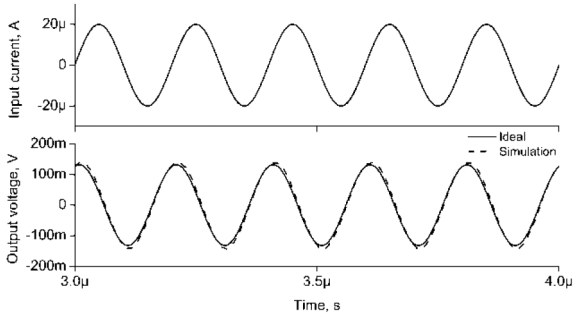

Fig. 17 *Time domain analysis for the proposed series lossy SF*

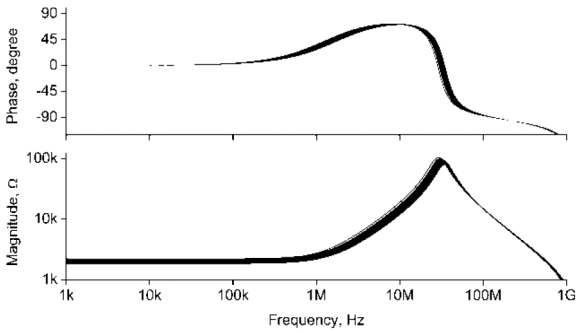

Fig. 18 *AC MC analysis with 100 runnings for the proposed series lossy SFI*

4 Parasitic impedance effects

DDCC− with its X, $Z-$, Y_1, Y_2 and Y_3 terminal parasitic impedances is denoted in Fig. 14. if only parasitic impedances are considered, DDCC− in Fig. 14 can be defined as in the following matrix equation:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & R_X & 0 \\ sC_{Y1} & 0 & 0 & 0 & 0 \\ 0 & sC_{Y2} & 0 & 0 & 0 \\ 0 & 0 & sC_{Y3} & 0 & 0 \\ 0 & 0 & 0 & -1 & sC_{Z-} + 1/R_{Z-} \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_{Z-} \end{bmatrix} \tag{26}$$

As an example, parasitic impedance effects on the performance of the proposed negative lossless SFI are investigated. If the second

Table 1 Aspect ratios of the MOS transistors of the DDCC− in Fig. 15

PMOS transistors	W(μm)/L(μm)
M_1–M_{10}	40/0.5
NMOS transistors	W(μm)/L(μm)
M_{11}–M_{16}	13/0.5

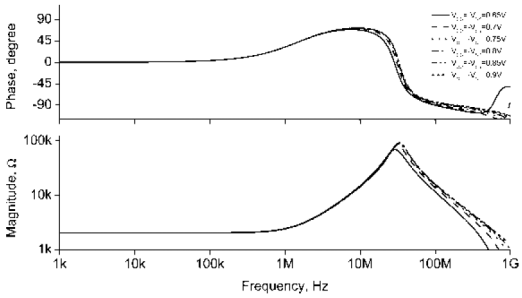

Fig. 19 *AC analysis with supply voltage changes for the proposed series lossy SFI*

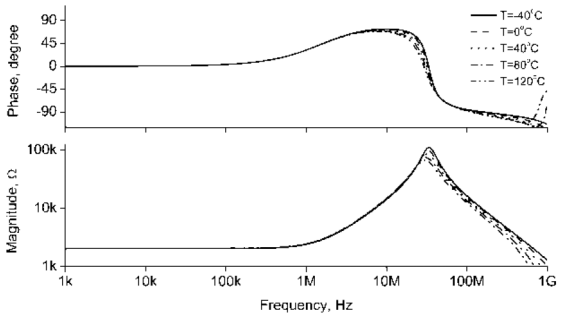

Fig. 20 *AC analysis with temperature variations for the proposed series lossy SFI*

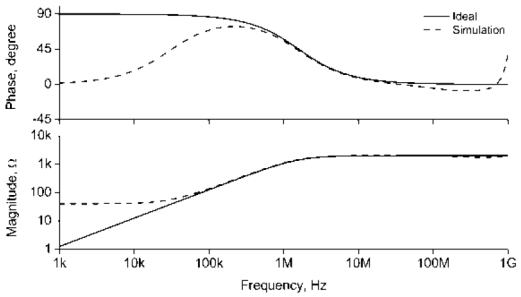

Fig. 21 *AC analysis for the proposed parallel lossy SFI*

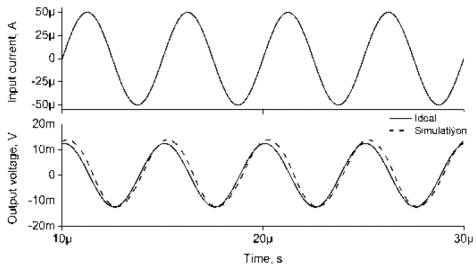

Fig. 22 *Time domain analysis for the proposed parallel lossy SFI*

terminal of the proposed negative lossless SFI is grounded, the input impedance due to parasitic impedances is evaluated as

$$Z_{\text{in1}} = \frac{1}{sC_{Y1}} // \frac{R_X(1 + s(C + C_{Y3})(R_1 + R_2)) + s(C + C_{Y3})R_1R_2}{-1 + s(C + C_{Y3})R_X} \quad (27)$$

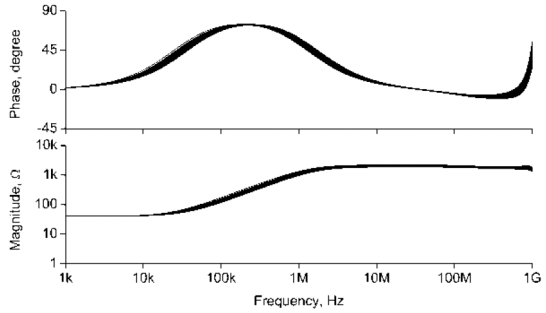

Fig. 23 *AC MC analysis with 100 runnings for the proposed parallel lossy SFI*

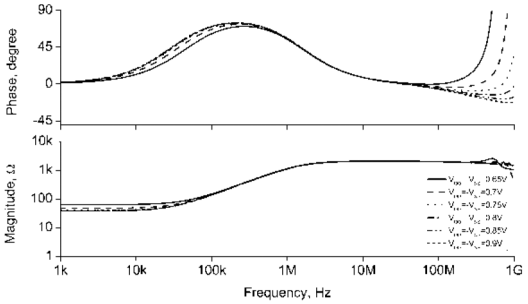

Fig. 24 *AC analysis with supply voltage changes for the proposed parallel lossy SFI*

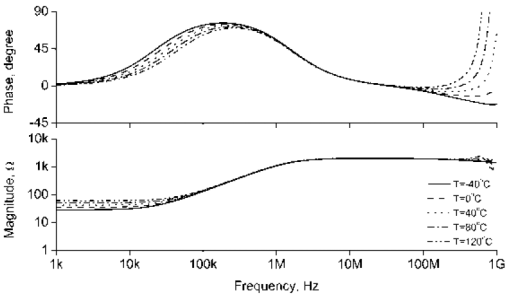

Fig. 25 *AC analysis with temperature variations for the proposed parallel lossy SFI*

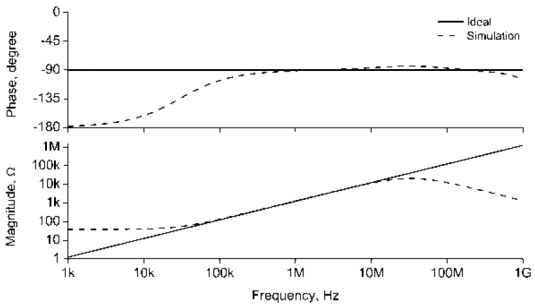

Fig. 26 *AC analysis for the proposed negative lossless SFI*

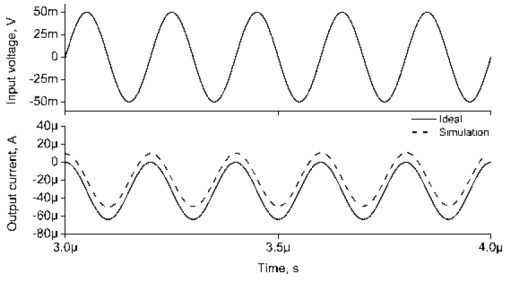

Fig. 27 *Time domain analysis for the proposed negative lossless SFI*

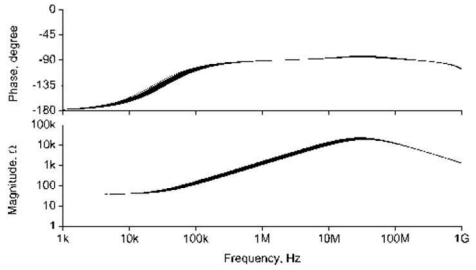

Fig. 28 *AC MC analysis with 100 runnings for the proposed negative lossless SFI*

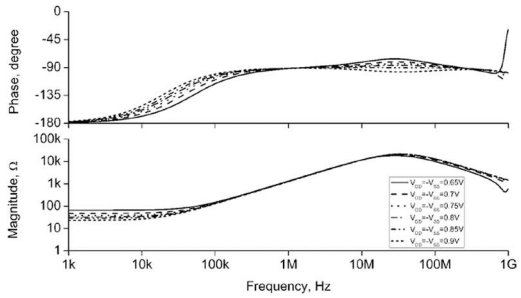

Fig. 29 *AC analysis with supply voltage changes for the proposed negative lossless SFI*

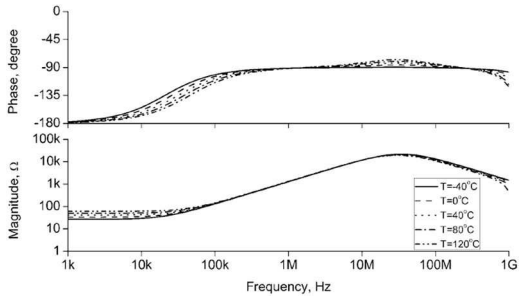

Fig. 30 *AC analysis with temperature variations for the proposed negative lossless SFI*

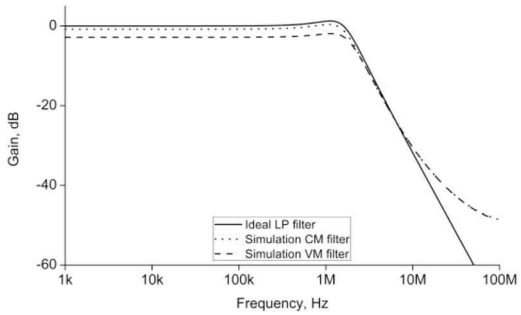

Fig. 31 *Gain responses of the CM and VM LP filters*

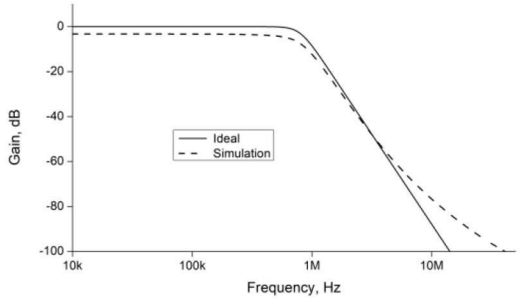

Fig. 32 *Gain responses of the fourth-order CM Butterworth LP filter in Fig. 10*

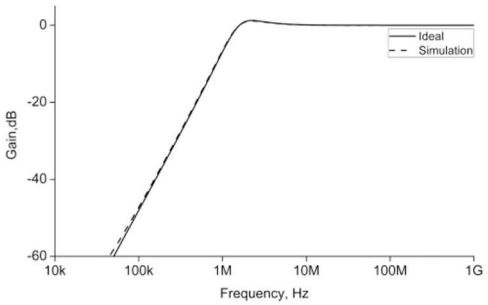

Fig. 33 *Gain responses of the CM HP filter*

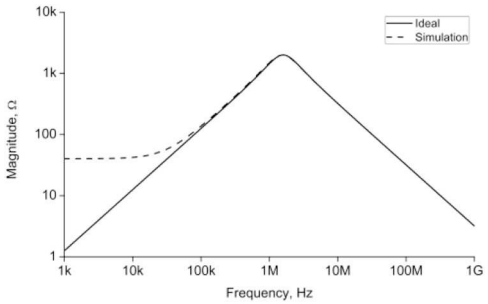

Fig. 34 *Magnitudes of the impedance of the RLC resonant circuit*

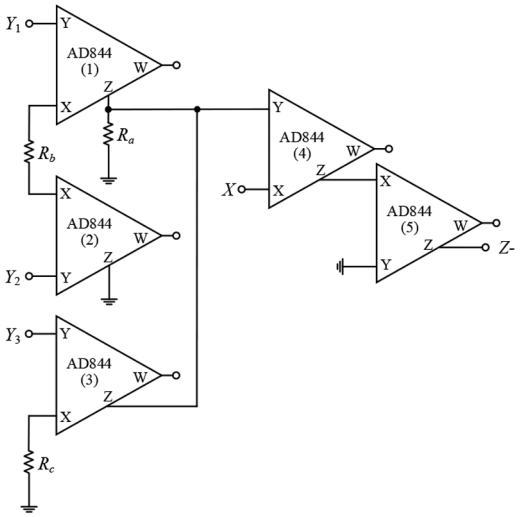

Fig. 35 *DDCC− realisation with five AD844s [55] and three identical resistors*

If the first terminal of the proposed negative lossless SFI is grounded, the input impedance due to parasitic impedances is calculated as

$$Z_{in2} = \frac{1}{s(C_{Z-} + C_{Y2}) + (1/R_{Z-})} // Z(s) \tag{28}$$

Here, $Z(s)$ is found as

$$Z(s) = \frac{R_X(1 + s(C + C_{Y3})(R_1 + R_2)) + s(C + C_{Y3})R_1R_2}{-1 - sC_{Y3}(R_1 + R_2) + sCR_X + s^2CC_{Y3}(R_1R_2 + R_X(R_1 + R_2))} \tag{29}$$

5 Simulation results

MOS transistor based DDCC− in Fig. 15 is derived from [4]. Supply voltages and a bias voltage of the DDCC− are chosen as ±0.75 V and $V_B = 0.23$ V, respectively. Dimensions of all the MOS transistors of the DDCC− in Fig. 15 are denoted in Table 1. Parasitic impedances, $R_X \cong 30\ \Omega$, $R_{Z-} \cong 11$ kΩ, $C_{Z-} \cong 30$ fF, $C_{Y1} = C_{Y2} \cong 105$ fF and $C_{Y3} \cong 8$ fF are found via SPICE program. In

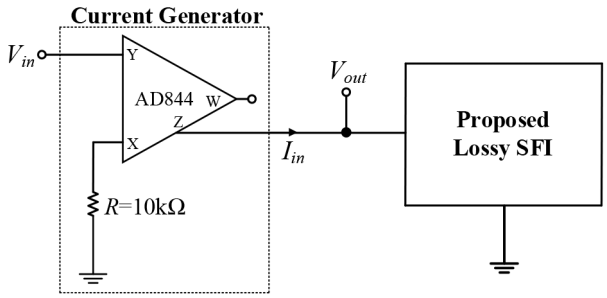

Fig. 36 *Experimental setup for the proposed series and parallel lossy SFIs*

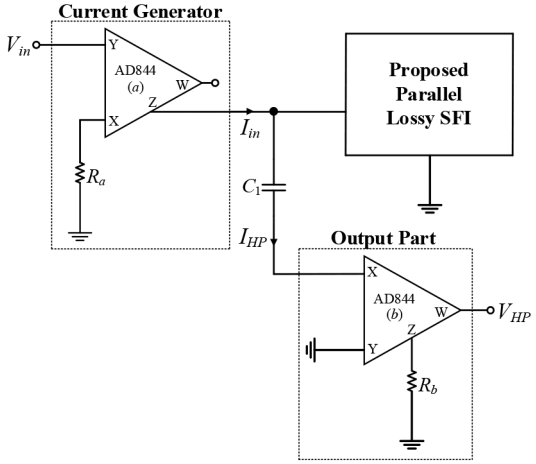

Fig. 37 *Presented HP filter realised with the proposed parallel lossy SFI along with extra two AD844s, two resistors and one capacitor*

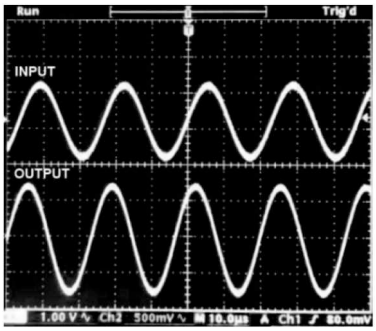

Fig. 38 *Input and corresponding output for the proposed series lossy SFI*

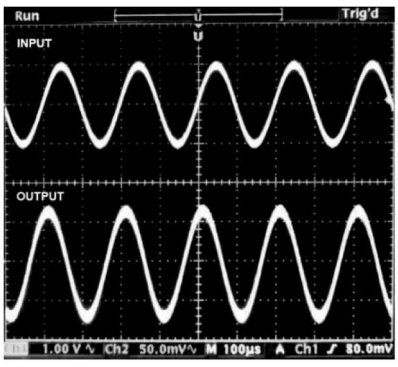

Fig. 39 *Input and corresponding output for the proposed parallel lossy SFI*

addition, $\gamma_o \cong \beta_{1o} \cong \beta_{2o} \cong \beta_{3o} \cong 0.99$, $f_\gamma \cong 1.67$ GHz, $f_{\beta 1} \cong 2.25$ GHz, $f_{\beta 2} \cong 2.2$ GHz and $f_{\beta 3} \cong 2.8$ GHz are found. Apart from these, passive elements, $R_1 = 1$ kΩ, $R_2 = 4$ kΩ and $C = 50$ pF are chosen for the series lossy SFI; thus, $L_{eq} = 200$ µH and $R_{eq} = 2$ kΩ are obtained. Passive elements, $R_1 = 4$ kΩ, $R_2 = 1$ kΩ and $C = 50$ pF are chosen for the parallel lossy SFI; accordingly, $L_{eq} = 200$ µH and

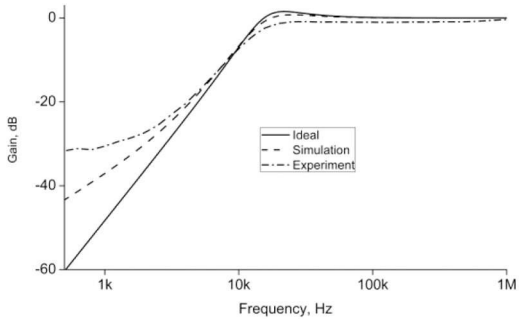

Fig. 40 *Ideal, simulation and experimental test results of the HP filter*

$R_{eq} = 2$ kΩ are obtained. Furthermore, passive components, $R_1 = 2$ kΩ, $R_2 = 2$ kΩ and $C = 50$ pF are chosen for the negative lossless SFI; therefore, $L_{eq} = 200$ µH is obtained. All of the proposed SFIs are simulated through SPICE program. The power dissipation of the proposed series and parallel lossy SFIs given in Figs. 2 and 3 is found as 2.06 mW. Moreover, the power dissipation of the proposed negative lossless SFI given in Fig. 4 is found as 1.96 mW.

An AC analysis, a time domain analysis, an AC Monte Carlo (MC) analysis with 100 runnings, an AC analysis with supply voltage changes and an AC analysis with temperature variations for the proposed series lossy SFI are shown in Figs. 16–20, respectively. An AC analysis, a time domain analysis, an AC MC analysis with 100 runnings, an AC analysis with supply voltage changes and an AC analysis with temperature variations for the proposed parallel lossy SFI are shown in Figs. 21–25, respectively. An AC analysis, a time domain analysis, an AC MC analysis with 100 runnings, an AC analysis with supply voltage changes and an AC analysis with temperature variations for the proposed lossless negative SFI are shown in Figs. 26–30, respectively. Magnitudes and phases of the impedances are given in all the AC analyses. In time domain analyses, 20 µA peak input current at 5 MHz is applied to the input of the proposed series lossy SFI, 50 µA peak input current at 200 kHz is applied to the input of the proposed parallel lossy SFI and 50 mV peak input voltage is applied to the input of the proposed negative lossless SFI. DC supply voltages are varied from ±0.65 to ±0.9 V by an increment of 50 mV in Figs. 19, 24 and 29. Temperatures are varied from −40 to 120°C by an increment of 40°C in Figs. 20, 25 and 30. Also, the values of all the passive elements are uniformly varied with 10% in MC simulations.

One can observe from Figs. 18–20, 23–25 and 28–30 that phases and magnitudes of the impedances a bit change due to MC analyses, supply voltage variations and temperature variations. Moreover, simulation results are close to ideal ones but an unimportant difference between them can be attributed to non-idealities of the DDCC in Fig. 15. These non-idealities are parasitic impedances and frequency-dependent non-ideal gains.

Gain responses of the CM and VM LP filters are given in Fig. 31 in which passive elements, $R_1 = 1$ kΩ, $R_2 = 4$ kΩ and $C_1 = C_2 = 50$ pF are chosen for the CM and VM LP filters, respectively, shown in Figs. 8 and 9; thus, $Q = 1$ and $f_o \cong 1.59$ MHz are obtained. Gain responses of the fourth-order CM Butterworth LP filter in Fig. 10 are shown in Fig. 32 where the passive elements,

Table 2 Comparisons of the open literature SIs [9–38] and the proposed ones

References	No. of capacitors		No. of resistor		Use more than one Z terminal	Type of active devices (No. of active devices)	Technology	Matching condition
	Grounded	Floating	Grounded	Floating				
[9] in Fig. 3	1	0	2	0	yes	DVCC (2)	NA	no
[10] in Figs. 5–11	1	0	1–3	0 or 1	yes	DVCC/ DDCC (2–3)	0.35 μm	yes
[11] in Fig. 16	1	0	2	0	yes	DVCC (2)	NA	no
[12] in Fig. 2	1	0	2	0	yes	DVCC (2)	0.35 μm	no
[13] in Fig. 1	1	0	1	1	no	DVCC (2)	0.18 μm	no
[14] in Fig. 2	1	0	1	1	yes	DDCC (2)	0.13 μm	no
[14] in Fig. 3	1	0	0	2	yes	DDCC (2)	0.13 μm	no
[15] in Fig. 3	1	0	1	1	yes	DVCC (3)	0.5 μm	no
[16] in Fig. 4	1	0	2	0	yes	DDCC (1)	0.13 μm	yes
[16] in Fig. 5	1	0	2	0	yes	DDCC (1)	0.13 μm	yes
[17] in Fig. 2	0 or 1	0 or 1	0 or 1	1 or 2	yes	DVCC (1)	0.18 μm	yes
[17] in Fig. 3	0 or 1	0 or 1	0 or 1	1 or 2	yes	DDCC (1)	0.18 μm	yes
[17] in Figs. 4–6	0	1	0	2	no	DDCC (1)	0.18 μm	yes
[18] in Fig. 2	1	0	1	1	yes	DDCC (1)	0.35 μm	no
[19] in Fig. 1	1	0	1	1	yes	CCII (3)	0.35 μm	no
[20] in Fig. 1	1	0	1	1	yes	CCII (2)	BJT	no
[21] in Fig. 1	2	0	0	2	no	CCII (4)	AD844	no
[22] in Fig. 1	1	0	3	0	yes	CCII (3)	0.35 μm	yes
[23] in Fig. 1a	1	0	1	1	yes	CCII (2)	NA	no
[24] in Fig. 1	1	0	0	2	no	CCII (4)	BJT	no
[25] in Fig. 1	0	2	0	3	no	CFOA (2)	AD844	yes
[26] in Fig. 1a	0	1	0	2	no	CFOA (2)	AD844	no
[27] in Fig. 1	0	1	0	2	no	CFOA (2 or 3)	AD844	no
[28] in Fig. 3b	1	0	0	2	no	CFOA (3)	AD844	no
[29] in Fig. 1	1	0	2	2	no	CFOA (4)	AD844	no
[30] in Fig. 3	1	0	0	0	no	CC-CFA (3)	BiCMOS	no
[31] in Fig. 3	1	0	0	0	yes	ZC-CFCCC (2)	0.18 μm	yes
[32] in Fig. 3b	1	0	1	0	no	CBTA (1)	0.25 μm	no
[33] in Figs. 2, 3	0	1	0	1	no	VDBA (1)	0.25 μm	no
[34] in Fig. 3a [a]	1	0	0	0	no	VDIBA (1)	0.25 μm	no
[34] in Fig. 3b [a]	0	1	0	0	no	VDIBA (1)	0.25 μm	no
[35] in Figs. 3–5	1	0	0	1	no	VDDDA (2)	LM13700 and AD830	no
[36] in Figs. 2–4 [a]	0	1	1	0	no	LT1228 (1)	LT1228	no
[37] in Fig. 2	1	0	0	0	yes	CCCII (1), OTA (1)	BJT	no
[38] in Fig. 5	1	0	0	0	yes	DXCCTA (1)	0.18 μm	no
the first SFI	0	1	0	2	no	DDCC (1)	0.13 μm	no
the second SFI	0	1	0	2	no	DDCC (1)	0.13 μm	no
the third SFI	0	1	0	2	no	DDCC (1)	0.13 μm	no

NA: not available.

[a]GSI.

$R_1 = 1.848$ kΩ, $R_2 = 2.164$ kΩ, $R_3 = 765.7$ Ω, $R_4 = 5.224$ kΩ and $C_1 = C_2 = C_3 = C_4 = 100$ pF yielding $f_0 \cong 795.75$ kHz are chosen. Gain responses of the CM HP filter in Fig. 11 are depicted in Fig. 33 where the passive elements, $R_1 = 4$ kΩ, $R_2 = 1$ kΩ and $C_1 = C_2 = 50$ pF are chosen for the CM HP filter; accordingly, $Q = 1$ and $f_o \cong 1.59$ MHz are obtained. Magnitudes of the impedance of the RLC resonant circuit are demonstrated in Fig. 34 where the passive components, $R_1 = 4$ kΩ, $R_2 = 1$ kΩ and $C_1 = C_2 = 50$ pF are chosen; accordingly, $Q = 1$ and $f_o \cong 1.59$ MHz are obtained.

6 Experimental results

The DDCC− can be implemented with five AD844s [55] and three identical resistors, $R_a = R_b = R_c = 2.2$ kΩ to perform experiments, which is given in Fig. 35. In order to perform experiments for the proposed series and parallel lossy SFIs, the experimental set up in Fig. 36 is used. Furthermore, the experimental set up in Fig. 37 is used for the CM HP filter. Supply voltages of all the AD844s for all the experimental studies are chosen as ±9 V. Passive elements for the series lossy SFI are chosen as $R_1 = 1$ kΩ, $R_2 = 4.4$ kΩ and $C = 4.7$ nF resulting in $L_{eq} \cong 20.7$ mH and $R_{eq} = 2$ kΩ. Passive components for the parallel lossy SFI are chosen as $R_1 = 4.4$ kΩ, $R_2 = 1$ kΩ and $C = 4.7$ nF yielding $L_{eq} \cong 20.7$ mH and $R_{eq} = 2.2$ kΩ. An input current signal with 100 μA peak ($V_{in} = 1$ V peak input voltage) at 43 kHz is applied to the input of the proposed series lossy SFI. Also, input and corresponding output for the proposed series lossy SFI are shown in Fig. 38. An input current signal with 100 μA peak at 5 kHz is applied to the input of the proposed parallel lossy SFI. Further, input and corresponding output for the proposed parallel lossy SFI are given in Fig. 39. Passive components of the CM HP filter example in Fig. 37 are chosen as $R_1 = 4.4$ kΩ, $R_2 = 1$ kΩ, $R_a = R_b = 2.2$ kΩ and $C_1 = C_2 = 4.7$ nF resulting in $f_0 \cong 16.1$ kHz and $Q \cong 1$. In Fig. 40, ideal, simulation and experimental results of the VM HP filter example are shown. On the other hand, TF of the VM HP filter example is computed as

$$\frac{V_{HP}}{V_{in}} = \frac{R_b}{R_a} \frac{s^2 C_1 C_2 R_1 R_2}{s^2 C_1 C_2 R_1 R_2 + 2sC_2 R_2 + 1} \tag{30}$$

Comparisons of the open literature SIs [9–38] and the proposed ones are given in Table 2.

7 Conclusion and suggestions

Single DDCC− based three SFI circuits are proposed. These circuits are series lossy, parallel lossy and negative lossless SFIs. As application examples, second-order CM and VM LP filter circuits as well as a fourth-order CM Butterworth LP filter topology derived from the proposed series lossy SFI are presented. In addition, a second-order HP filter circuit and an RLC resonant circuit derived from the proposed parallel lossy SFI circuit are given. Non-ideality analyses are also given. Simulations of all the proposed circuits and application examples are accomplished via SPICE program. Moreover, some experiments are performed in this paper. Ideal, simulation and experimental results are coherent but the difference among them arises from non-idealities of the active devices.

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