

## Article

# A New Simulated Inductor with Reduced Series Resistor Using a Single VCII±

Erkan Yuce <sup>1</sup>, Leila Safari <sup>2</sup>, Shahram Minaei <sup>3</sup>, Giuseppe Ferri <sup>2</sup> , Gianluca Barile <sup>2</sup>  and Vincenzo Stornelli <sup>2,\*</sup> 

<sup>1</sup> Department of Electrical and Electronics Engineering, Pamukkale University, Denizli 20160, Turkey; erkanyuce@yahoo.com

<sup>2</sup> Department of Industrial and Information Engineering, University of L'Aquila, 67100 L'Aquila, Italy; leilasafari@yahoo.com (L.S.); giuseppe.ferri@univaq.it (G.F.); gianluca.barile@univaq.it (G.B.)

<sup>3</sup> Department of Electrical and Electronics Engineering, Dogus University, Istanbul 34775, Turkey; sminaei@dogus.edu.tr

\* Correspondence: vincenzo.stornelli@univaq.it

**Abstract:** This paper presents a new realization of a grounded simulated inductor using a single dual output second-generation voltage conveyor (VCII±) as an active building block, two resistors and one grounded capacitor. The main characteristic of the proposed circuit is that the value of the series resistor can be significantly reduced. Thus, it has the property of improved low-frequency performance. Another feature is the use of a grounded capacitor that makes the proposed circuit attractive for integrated circuit (IC) realization. A simple CMOS implementation of the required VCII± is used. However, a single passive component-matching condition is required for the proposed structure. As an application example, a standard fifth-order high-pass ladder filter is also given. SPICE simulations using 0.18 μm CMOS technology parameters and a supply voltage of ±0.9 V as well as experimental verifications, are carried out to support the theory.

**Keywords:** simulated inductor; low-series resistor; VCII; voltage conveyor; high-gain VCII; current-mode; ladder filter; band-pass filter



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## 1. Introduction

Inductors are analog passive components that play an essential role in many analog and mixed-signal circuits. Due to the large occupation of area and the low-quality factor of spiral inductors, designers prefer to substitute them with simulated inductors (SIs) [1–49]. SIs are constructed using a few active elements, resistors and one capacitor, and exhibit characteristics of inductance within a specified frequency range. They find wide applications in the design of active filters, oscillators, phase shifters, etc. SIs using various kind of active devices offer some advantages such as the capability for integration, low area, high quality factor, operation in a wide frequency range, etc. However, grounded SIs [1–49] have the following problems. Some of the grounded SIs [1,2] use operational amplifiers (OAs); therefore, they suffer from slew-rate limitations. Other grounded SIs [1–10,12–14,19,21,31,33,34,39,48,49] employ more than one active building block (ABB). The grounded SI configurations described in [1,2,6,11,12,15–20,24–28,35,37,39,43–47] include a floating capacitor that is not suitable for integrated circuit (IC) fabrication. The grounded SI proposals in [17,22,24–30,36,38,42,45,46] contain complex internal structures. Other grounded topologies [40–46] are made up of non-standard active devices. Finally, the grounded SI architectures reported in [9,23,30–35,37] have a capacitor connected to a low-impedance terminal or consist of an operational transconductance amplifier (OTA); accordingly, their high-frequency performances are limited [50,51].

A literature survey revealed that, in recent years, the current-mode (CM) approach has been widely used in the SI design [1–17,20–22,24–29,36,38–49]. The main reason is the potential of the CM signal processing with its low-voltage nature and high-frequency

operation, etc. [52,53]. Recently, a new CM active building block called second-generation voltage conveyor (VCII) [54–56] has been used in the implementation of high-performance grounded immittance-function simulators [48,57]. This new block is the dual circuit of the more famous second-generation current conveyor (CCII). The difference between CCII and VCII is that, unlike VCII, CCII lacks a low-impedance voltage output port. This feature enables VCII-based circuits to benefit from advantages of processing signals in the current domain while producing output signals in voltage form. Therefore, VCII is suitable for all applications requiring output signal in the form of voltage. The results reported in [54–56] reveal that VCII-based circuits outperform conventional circuits in many aspects. For instance, achieved simulated impedances in [48,57] are robust against process mismatches and temperature variations while their power consumption is reduced, when compared to the other reported work. The latter feature comes from the very simple internal structure of the used ABB, i.e., VCII. The maximum operation frequency range and parasitic series impedance of the VCII-based grounded SI reported in [48] are 2.5 MHz and 191  $\Omega$ , respectively. It also employs two ABBs.

Here, we aim to design a VCII-based grounded SI with improved performance that uses only one ABB. The proposed circuit is based on one dual-output VCII (VCII $\pm$ ) as ABB, two resistors and one grounded capacitor. The most important feature of the new implementation is that the value of series impedance is considerably reduced by adjusting resistor values. Hence, it has the property of improved low-frequency performance. It employs only a grounded capacitor that results in easy integration in the IC process. In addition, the frequency range is extended to 10 MHz. Additionally, complete circuit analysis and SPICE simulation results are reported. As an application example, a fifth-order high-pass (HP) ladder filter is presented. Nevertheless, there is a simple matching condition which can be easily satisfied. Fortunately, this matching condition is also useful in setting the value of parasitic series resistance to the desired value. The promising results through the SPICE simulation program and experimental verifications show that VCII $\pm$  are highly suitable in the SI applications. Compared to the grounded SI based on the negative-impedance converters (NICs) of [49] which employ two active elements, two resistors and one grounded capacitor, the realized inductor value is four times lower than the one extracted from the proposed circuit for the same values of the capacitor and resistors.

The organization of this paper is as follows. In Section 2, VCII $\pm$  and the proposed SI are introduced and analyzed. The non-ideal analysis is performed in Section 3. Simulation results are reported in Section 4. Experimental verifications are presented in Section 5. Finally, Section 6 concludes the paper.

## 2. The Proposed Circuit

Figure 1 shows the symbolic presentation and internal structure of the VCII $\pm$  without a Z $-$  port. It has a low-impedance current input Y terminal, two high-impedance current output X $+$  and X $-$  terminals and one low impedance voltage output terminal, Z $+$ . It simply consists of a current buffer (CB) and a voltage buffer (VB). The input current is transferred from the Y terminal to the X $+$  terminal in the same direction and the X $-$  terminal in the opposite direction. The voltage at the X $+$  terminal is transferred to the Z $+$  terminal. The VCII $\pm$  demonstrated in Figure 1 is described as:

$$\begin{bmatrix} I_{X+} \\ I_{X-} \\ V_Y \\ V_{Z+} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta \\ 0 & 0 & -\eta \\ 0 & 0 & 0 \\ \alpha & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{X+} \\ V_{X-} \\ I_Y \end{bmatrix} \quad (1)$$

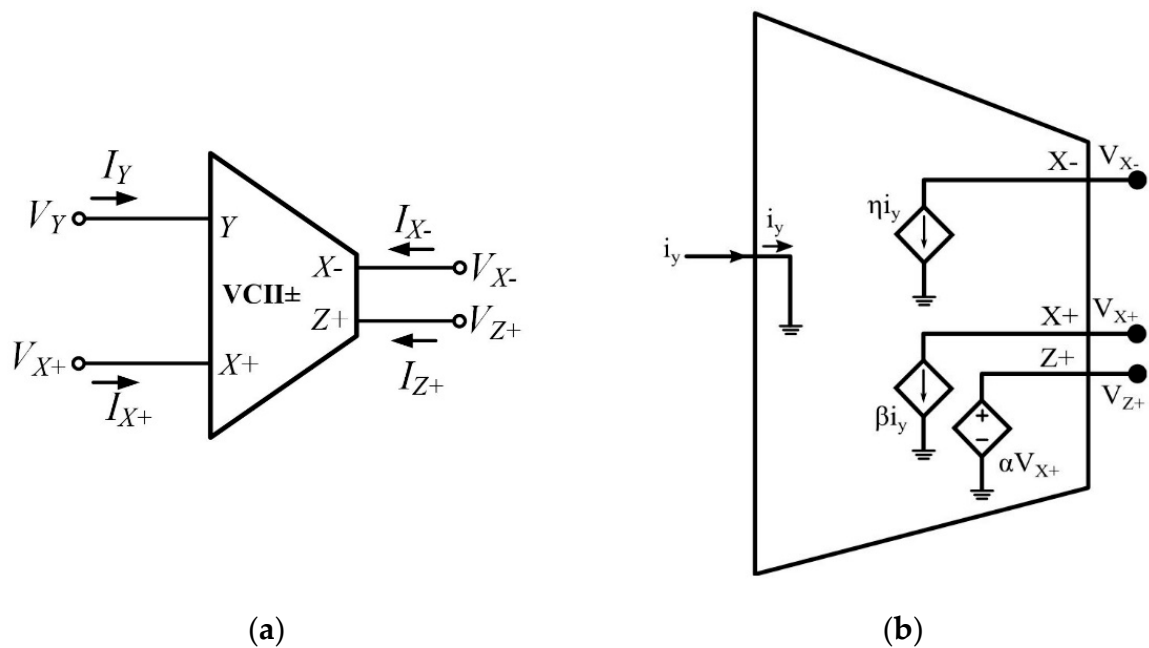


Figure 1. VCII± without Z− port: (a) symbolic presentation (b) internal structure.

In Equation (1),  $\beta$  and  $\eta$ , being current gains, are ideally equal to one and two, respectively. Additionally,  $\alpha$ , being voltage gain, is ideally equal to unity.

The proposed VCII±-based SI is shown in Figure 2. Simple analysis shows that, in the case of ideal VCII (negligible contribution of parasitic impedances), the input impedance of the proposed SI is evaluated by

$$Z_{in}(s) = sCR_1R_2 + R_1 - R_2 \tag{2}$$

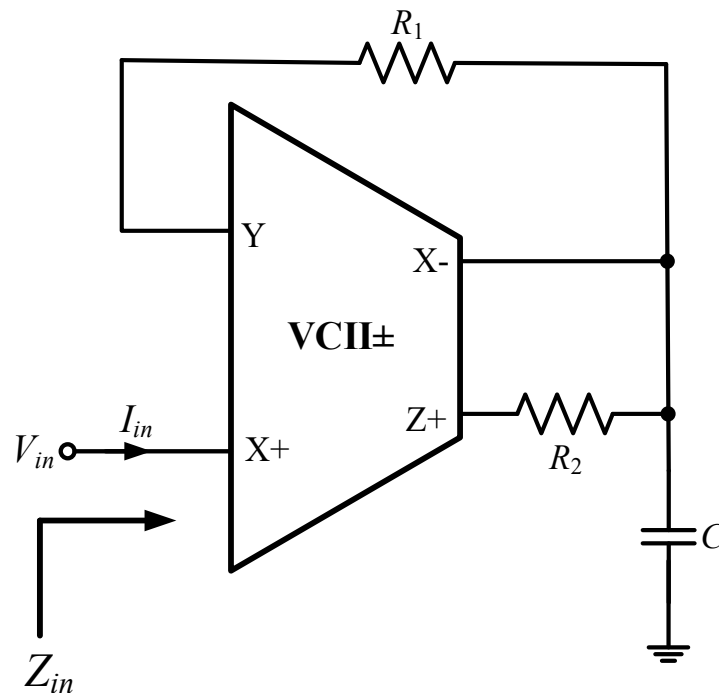


Figure 2. Proposed VCII±-based simulated inductor.

In above equation, if  $R_2 = R_1 = R$  is chosen, the following input impedance is obtained:

$$Z_{in}(s) = sCR^2 \tag{3}$$

One observes from Equation (3) that a positive lossless grounded SI is obtained. If non-ideal gains are considered, Equation (2) turns to:

$$Z_{in}(s) = \frac{sCR_1R_2 + R_1 + (1 - \eta)R_2}{\alpha\beta} \tag{4}$$

From Equation (4), quality factor (Q) for equivalent inductance is found as

$$Q = \left| \frac{\omega CR_1R_2}{R_1 + (1 - \eta)R_2} \right| \tag{5}$$

From Equation (5) it can be realized that for the ideal case, where  $R_1 = R_2$  and  $\eta = 2$ , the Q value of the inductance is infinity.

### 3. Parasitic Impedance Effects

Figures 3 and 4 show the  $VCII_{\pm}$  with its parasitic impedances and the equivalent model of the proposed SI, respectively. Thus, the  $VCII_{\pm}$  denoted in Figure 3 is described as

$$\begin{bmatrix} I_{X+} \\ I_{X-} \\ V_Y \\ V_{Z+} \end{bmatrix} = \begin{bmatrix} sC_{X+} + \frac{1}{R_{X+}} & 0 & 1 & 0 \\ 0 & sC_{X-} + \frac{1}{R_{X-}} & -2 & 0 \\ 0 & 0 & R_Y & 0 \\ 1 & 0 & 0 & R_{Z+} \end{bmatrix} \begin{bmatrix} V_{X+} \\ V_{X-} \\ I_Y \\ I_{Z+} \end{bmatrix} \tag{6}$$

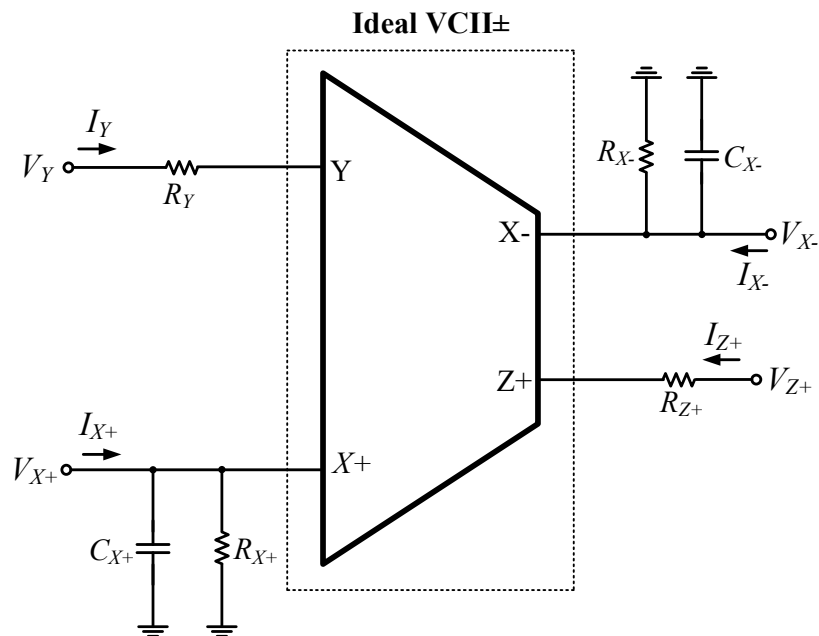


Figure 3.  $VCII_{\pm}$  and its parasitic impedances.

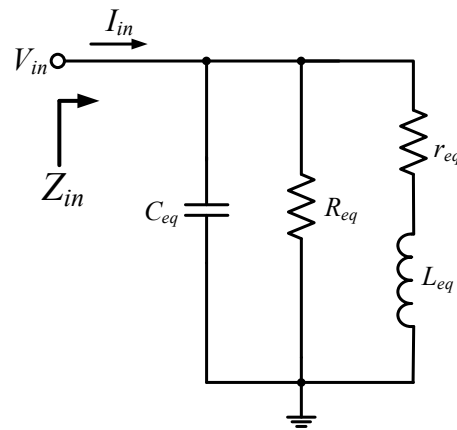


Figure 4. Equivalent model of the proposed simulated inductor.

By a simple analysis, including only parasitic impedances of the VCII $\pm$ , Equation (2) converts to:

$$Z_{in}(s) = R_{eq} // \frac{1}{sC_{eq}} // (sL_{eq} + r_{eq}) \quad (7)$$

Here,  $L_{eq}$ ,  $r_{eq}$ ,  $R_{eq}$  and  $C_{eq}$  are, respectively, calculated as

$$L_{eq} = (C + C_{X-})(R_1 + R_Y)(R_2 + R_{Z+}) \quad (8)$$

$$r_{eq} = \frac{(R_1 + R_Y) + (R_2 + R_{Z+})}{R_{X-}} + R_1 + R_Y - R_2 - R_{Z+} \quad (9)$$

$$R_{eq} = R_{X+} \quad (10)$$

$$C_{eq} = C_{X+} \quad (11)$$

It is seen from Equations (7) and (8) that the proposed SI has restrictions at high frequencies due to parasitic elements  $R_{X+}$  and  $C_{X+}$  and at low frequencies due to  $r_{eq}$ . Fortunately,  $r_{eq}$  can be set to zero by choosing  $R_2$  as follows:

$$R_2 = \frac{(R_1 + R_Y)R_{Z+} + (R_1 + R_Y - R_{Z+})R_{X-}}{R_{X-} - (R_1 + R_Y)} \quad (12)$$

If  $R_{X-}$  is too high ( $R_{X-} > \infty$ ), the Equation (12) is reduced to  $R_2 = R_1 + R_Y - R_{Z+}$ , which is easily satisfied in practice.

#### 4. Simulation Results

The performance of the proposed circuit of Figure 2 is tested through SPICE simulations using 0.18  $\mu\text{m}$  CMOS technology parameters and a supply voltage of  $\pm 0.9$  V. The resulted performance parameters for the VCII $\pm$ , derived from one in Figure 5 [58], are reported in Table 1 in which  $V_B = 0.23$  V is chosen. The proposed solution for the implementation of an equivalent inductor is not related to a specific VCII. The size of  $M_{13}$ ,  $M_9$ – $M_{10}$  determines the value of  $r_Y$ . The size of  $M_3$ ,  $M_{18}$  determines impedance at  $X+$  port; the size of  $M_8$ – $M_{24}$  determines the impedance at  $X-$  port; and finally the size of  $M_{11}$ – $M_{12}$ ,  $M_{14}$  determines the impedance at  $Z+$  port. Aspect ratios of the PMOS transistors,  $M_1$ – $M_7$  and  $M_9$ – $M_{12}$ , are chosen as  $40.5 \mu\text{m}/0.54 \mu\text{m}$  and  $M_8$ ,  $M_{13}$  and  $M_{14}$  are selected as  $81 \mu\text{m}/0.54 \mu\text{m}$ . Furthermore, those of NMOS transistors,  $M_{15}$ – $M_{23}$ , are chosen as  $13.5 \mu\text{m}/0.54 \mu\text{m}$  and that of  $M_{24}$  is selected as  $27 \mu\text{m}/0.54 \mu\text{m}$ . Total power-dissipation of the proposed SI is nearly found as 1.92 mW. To achieve an inductance value of about 200  $\mu\text{H}$ , all the values of passive components are chosen as  $R_1 = 2 \text{ k}\Omega$ ,  $R_2 \cong 2.16 \text{ k}\Omega$  and  $C = 50 \text{ pF}$ . Frequency responses of the proposed SI and an ideal inductor are shown in Figure 6. From the simulation results, the operation frequency range of the proposed SI

is 1 kHz–10 MHz. The value of series impedance is also obtained as a negligible value of 237 mΩ. To test the time-domain performance of the proposed inductor simulator, a sinusoidal input current with peak amplitude of 25 μA and frequency of 1 MHz is used.

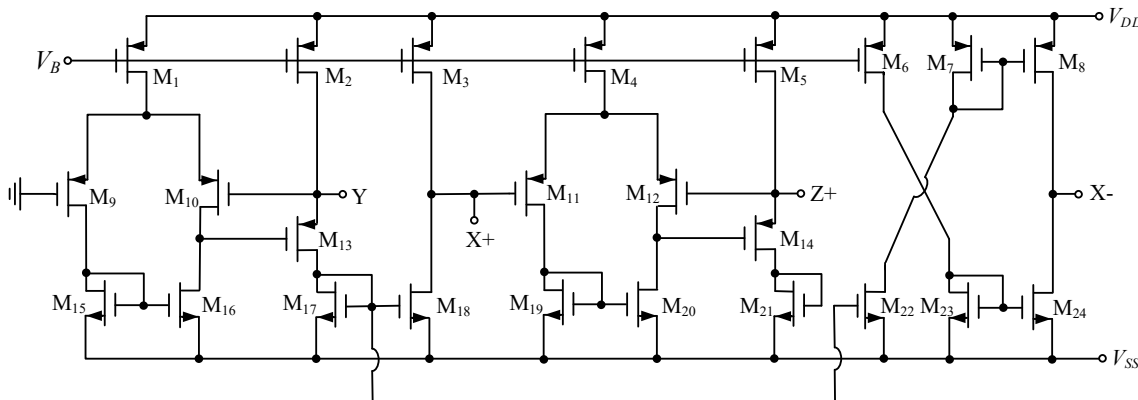


Figure 5. Internal structure of the used VCII± without Z− terminal.

Table 1. Some performance parameters of the VCII± of Figure 5.

Parameter	Value	Parameter	Value
$R_Y$	19 Ω	$\beta$	1.004
$R_{X+}$	41 kΩ	$\eta$	2.021
$R_{X-}$	20 kΩ	$\alpha$	0.973
$R_{Z+}$	19 Ω		
$C_{X+}$	143 fF		
$C_{X-}$	111 fF		

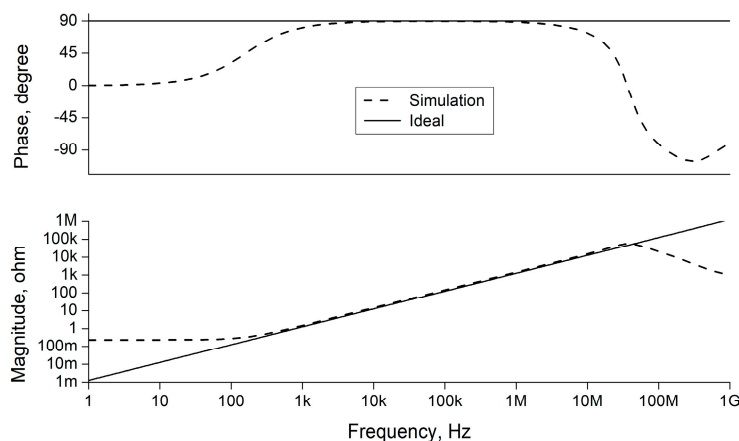


Figure 6. Frequency responses of the proposed simulated inductor and ideal inductor.

Figure 7 shows the produced output signals along with applied input signal. Additionally, the value of total harmonic distortion (THD) is 1.8%. The value of the phase shift between input current and output voltage is approximately 90°. There is an offset voltage at the simulation output voltage whose value is approximately −12 mV. Figure 8 shows the THD variations for various amplitudes of the peak-input currents at a frequency of 1 MHz. Favorably, the maximum value of THD remains below 3.7%. To test the frequency-domain applicability of the proposed SI, it is used in a standard fifth-order HP ladder filter shown in Figure 9 with  $L_{eq1} = L_{eq2} = 200 \mu\text{H}$ ,  $R_S = R_L = 5 \text{ k}\Omega$  and  $C_1 = C_2 = C_3 = 50 \text{ pF}$ . Frequency-domain analysis for the filter is given in Figure 10. A time-domain analysis for the filter example is depicted in Figure 11, in which a sinusoidal input voltage with a 250 mV peak and a frequency of 2.5 MHz is applied. Figure 12 demonstrates the THD variations for

various amplitudes of peak-input voltages at 2.5 MHz. Monte Carlo (MC) simulations are accomplished in 100 runs where all the passive elements of the filter, as shown in Figure 13, are changed by 1%. Furthermore, threshold voltages of all the MOS transistors in Figure 5 are varied by 1% and the result for the filter example is given in Figure 14. Power supplies are varied and the result for the filter example is depicted in Figure 15.

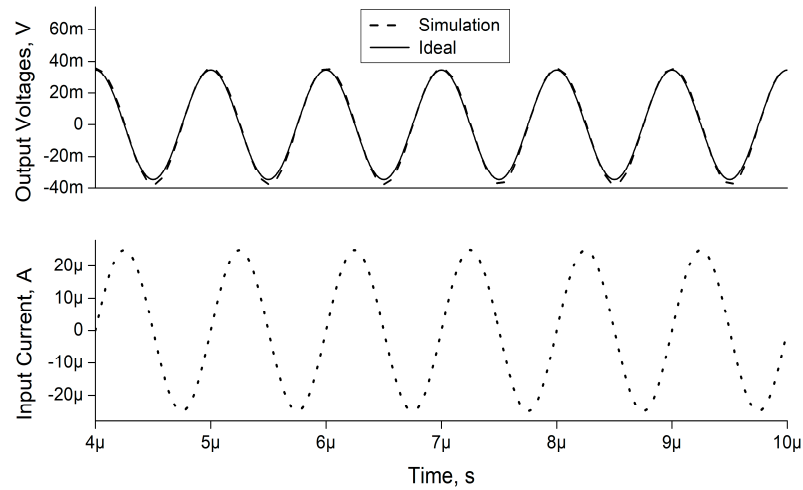


Figure 7. Time-domain responses of the proposed simulated inductor.

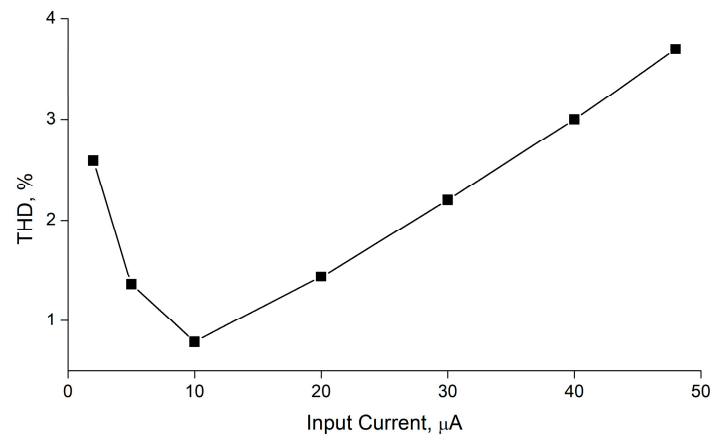


Figure 8. THD values of output voltages of the proposed simulated inductor for different peak values of the input currents.

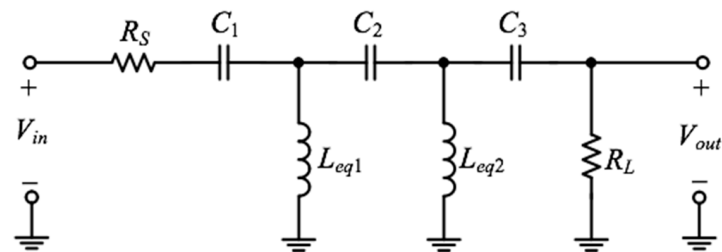


Figure 9. Standard fifth-order high-pass ladder filter realization [49].

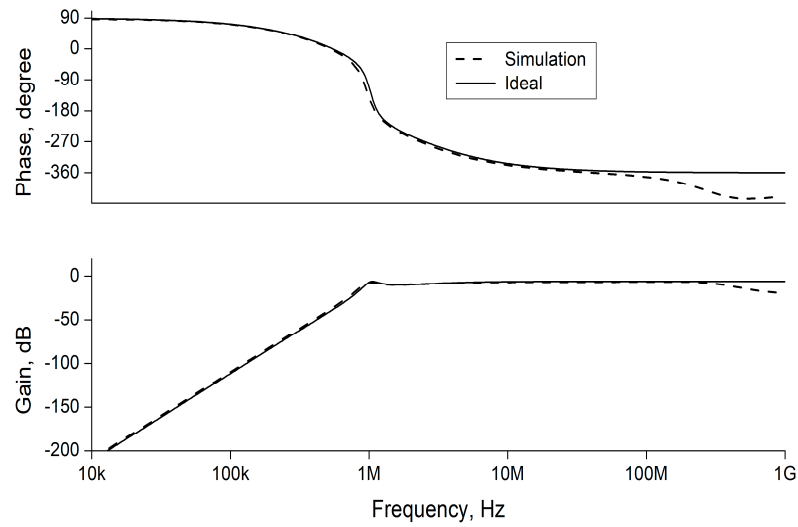


Figure 10. Frequency responses of the fifth-order high-pass ladder filter example.

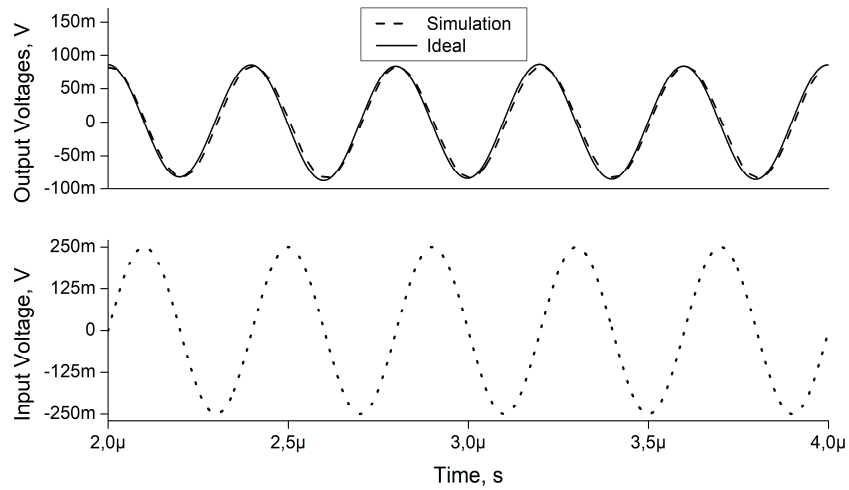


Figure 11. Time-domain analysis for the HP ladder filter example.

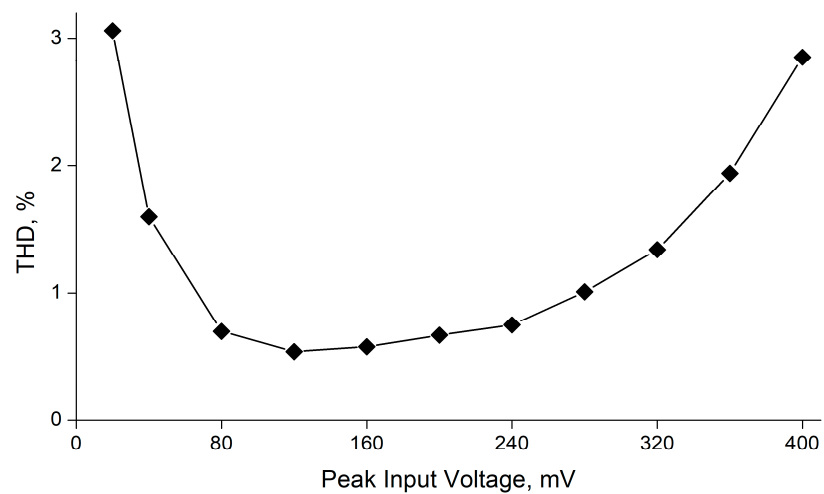


Figure 12. THD variations of the HP ladder filter for various amplitudes of the peak-input voltages at 2.5 MHz.



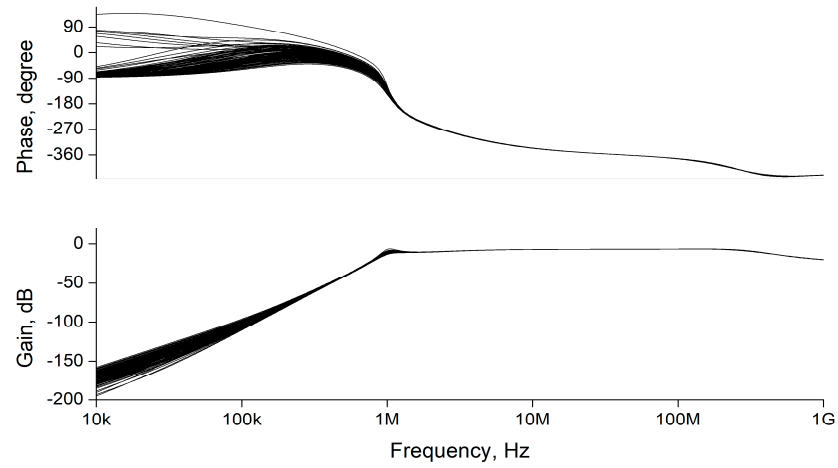


Figure 13. Monte Carlo simulations of the HP ladder filter with changes of all the passive elements.

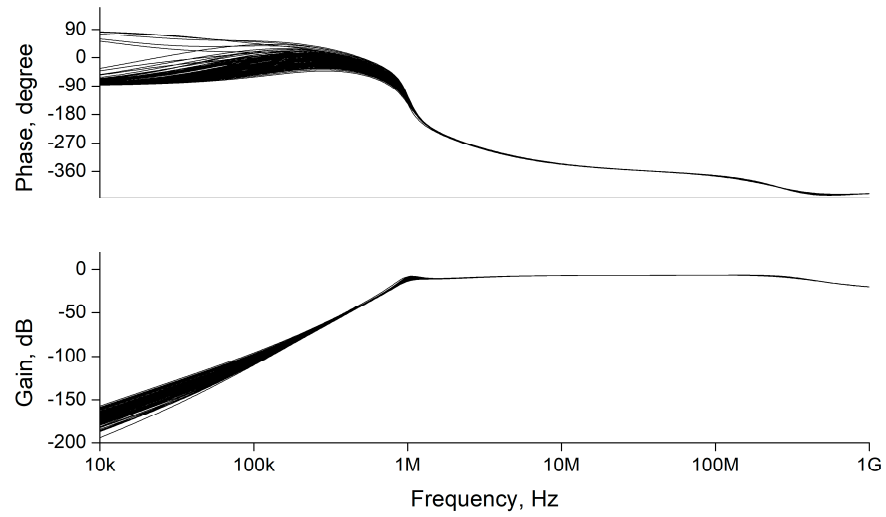


Figure 14. Monte Carlo simulations of the HP ladder filter with changes of threshold voltages of all the MOS transistors.

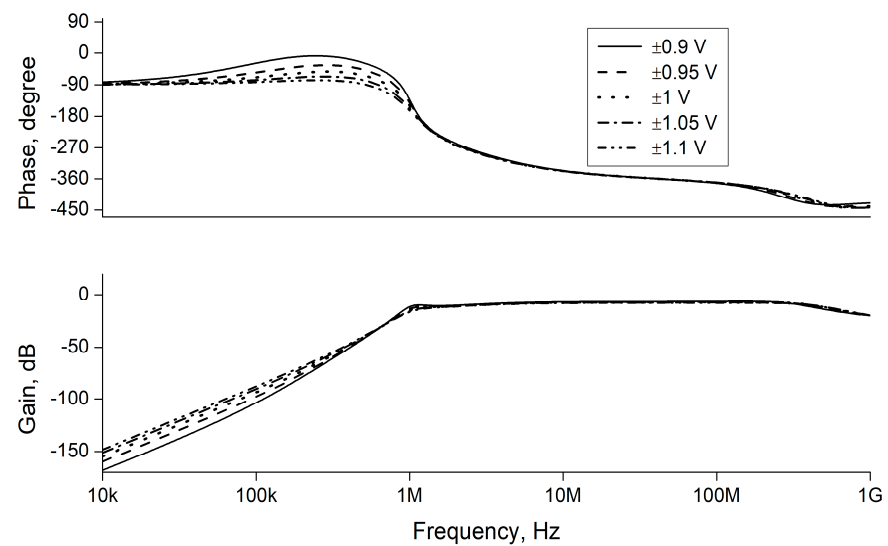


Figure 15. Frequency responses of the HP ladder filter for different power supplies.

A comparison among the proposed grounded SI with other reported similar works, such as CFOA [4–7], CCII [8–11] and VCII-based ones [47,48], is drawn in Table 2, which considers important parameters such as technology, power dissipation, supply voltage, frequency range and the number of grounded and floating passive components, etc. The work reported in [4] suffers from a high supply voltage of  $\pm 5V$ . Although the frequency range of the circuit reported in [7] is limited to 1 kHz, it consumes larger power consumption compared to the proposed circuit because it employs two CFOA as active building blocks. In fact, compared to VCII, which consists of one CB and one VB, the internal structure of each CFOA is formed by one CB and two VBs. Therefore, even in equal conditions, the circuit reported in [7] consumes larger power if compared to the proposed one. The circuit reported in [10], which employs three CCII as active building blocks, is applicable at frequencies larger than 100 kHz while the proposed circuit low-frequency range is 1 kHz. This is attributed to the reduced parasitic series resistance as well as its simplicity, which employs only one active building block; therefore, the number of parasitic elements, which are the frequency-performance limiting factor, is reduced. Although, compared to the previously reported VCII-based SI circuit of [48], the power consumption of the proposed circuit is increased approximately 3 times, but the frequency range is extended from 2.5 MHz to 10 MHz. The work reported in [48] also shows a lossy inductor. In addition, the series resistance is decreased from  $191 \Omega$  to  $0.23 \Omega$ . Moreover, by setting the values of  $R_1$  and  $R_2$ , the value of a parasitic series resistor can be set as required in the specific application.

**Table 2.** A comparison among the proposed circuit and some other previously reported similar works.

Reference	# ABB (Type)	# of Passive Elements		Frequency Range	Technology	Power Dissipation (mW)	VDD-VSS	Improved Low Frequency Performance
		# of R G (F)	# of C G (F)					
[4]	3 (CFOA)	2 (1)	1 (0)	1 $\mu$ Hz–1 MHz	AD844	NA	$\pm 5$	Yes
[5]	2 (CFOA)	1 (1)	1 (0)	NA	AD844	NA	NA	No
[6]*	1 (CFOA)	1 (1)	0 (1)	Low	AD844	NA	$\pm 15$	No
[7]	2 (CFOA)	2 (1)	1 (0)	1 kHz–100 MHz	0.13 $\mu$ m	3.05	$\pm 0.75$	Yes
[8]	2 (CCII)	2 (0)	1 (0)	NA	NA	NA	NA	No
[9]	2 (CCII)	2 (0)	1 (0)	NA	AD844	NA	$\pm 12$	No
[10]	3 (CCII)	2 (1)	1 (0)	100 kHz–100 MHz	0.35 $\mu$ m	NA	$\pm 1.5$	Yes
[11]	1 (CCII)	2 (2)	0 (1)	NA	NA	NA	NA	No
[47]*	MOS transistors	2 (0)	0 (1)	<1 kHz	NA	NA	NA	No
[48]	2 (VCII)	0 (2)	1 (0)	50 kHz–2.5 MHz	0.18 $\mu$ m	0.65	$\pm 0.9V$	No
Proposed	1 VCII $\pm$	0 (2)	1 (0)	1 kHz–10 MHz	0.18 $\mu$ m	1.92	$\pm 0.9V$	Yes

G: grounded, F: floating, NA: not available, \*: lossy.

## 5. Experimental Verifications

Implementation of the VCII $\pm$  by utilizing AD844s [59] is demonstrated in Figure 16 where supply voltages of AD844s are chosen as  $\pm 12 V$ . Additionally, passive elements  $R_a = R_b = 2.2 \text{ k}\Omega$ ;  $R_c = 1.1 \text{ k}\Omega$  for realizing VCII;  $R_1 = R_2 = 2.2 \text{ k}\Omega$ ; and  $C = 2.2 \text{ nF}$  for realizing  $L$ , are selected to obtain  $L_{eq} \cong 10.65 \text{ mH}$ . Figure 17 shows a picture of the fabricated board, highlighting its main features. The experimental setup used to evaluate the equivalent inductance is depicted in Figure 18 where  $R' = 1 \text{ k}\Omega$  is chosen. Thus, a time-domain analysis of the measured grounded SI is given in Figure 19, where a sinusoidal input voltage signal ( $V_{in}$ ) with 0.5 V peak at 25 kHz is applied to the input and output voltage taken from  $V_{out}$ . The measured phase shift between them is approximately  $86^\circ$ . A second-order voltage-mode band-pass (BP) filter application is analyzed as well: in Figure 20 the schematic that is used for this experiment is reported. Transfer function of the BP filter in Figure 20 is evaluated as:

$$H(s) = \frac{s \frac{1}{C_f R}}{s^2 + s \frac{1}{C_f R} + \frac{1}{LC_f}} \quad (13)$$

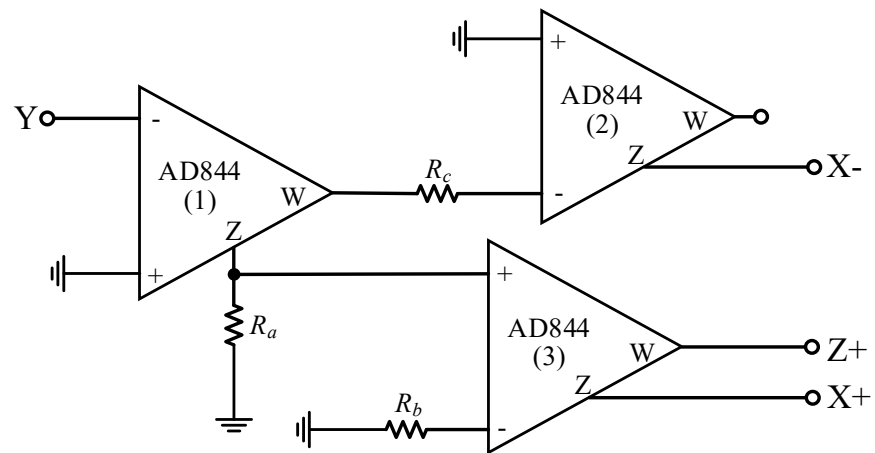


Figure 16. Implementation of the  $V_{CI\pm}$  by utilizing AD844s.

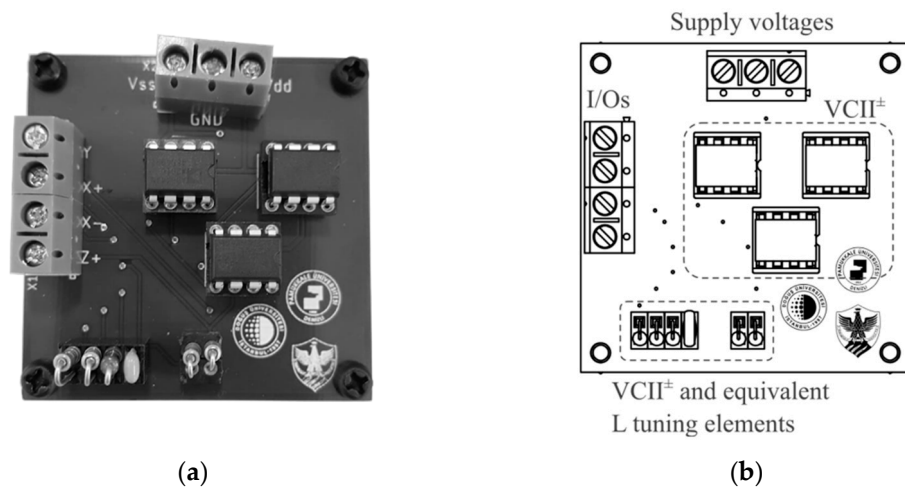


Figure 17. A photograph of the fabricated board (a) and its description (b).

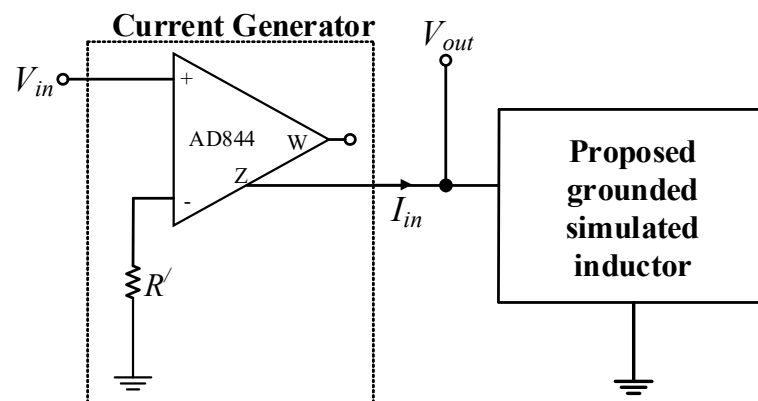


Figure 18. Experimental setup for realizing the grounded simulated inductor.

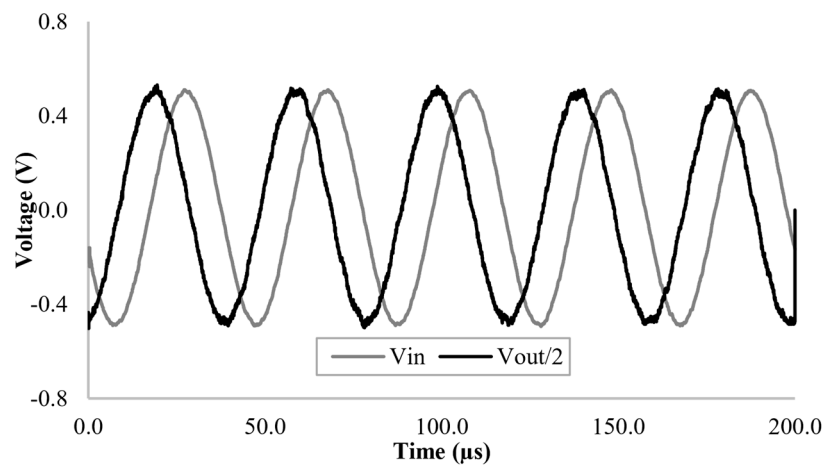


Figure 19. Measured time-domain analysis of the grounded simulated inductor.

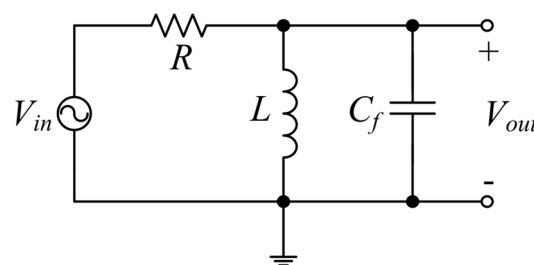


Figure 20. A second-order voltage-mode band-pass filter application.

The measured transfer function is reported in Figure 21 and compared to the simulated and the ideal ones. For this analysis the following values are chosen:  $R \cong 1 \text{ k}\Omega$ ,  $R_1 \cong 1.9 \text{ k}\Omega$  (given in order to improve low-frequency performance);  $R_2 = 2.2 \text{ k}\Omega$  and  $C = 2.2 \text{ nF}$ , yielding  $L \cong 9.2 \text{ mH}$ . Additionally,  $C_f = 30 \text{ nF}$  is chosen to obtain  $f_0 \cong 9.58 \text{ kHz}$ . In Figure 21, there is good agreement between ideal, simulated and measurement results above 1 kHz. Any discrepancy between these results occurs at frequencies below 1 kHz which is not in the operation frequency range of the proposed circuit and is due to the combined non idealities from AD844s. A time-domain analysis for the BP filter is given in Figure 22 in which a sinusoidal input voltage with 1 V peak-to-peak at  $f = f_0$  is applied.

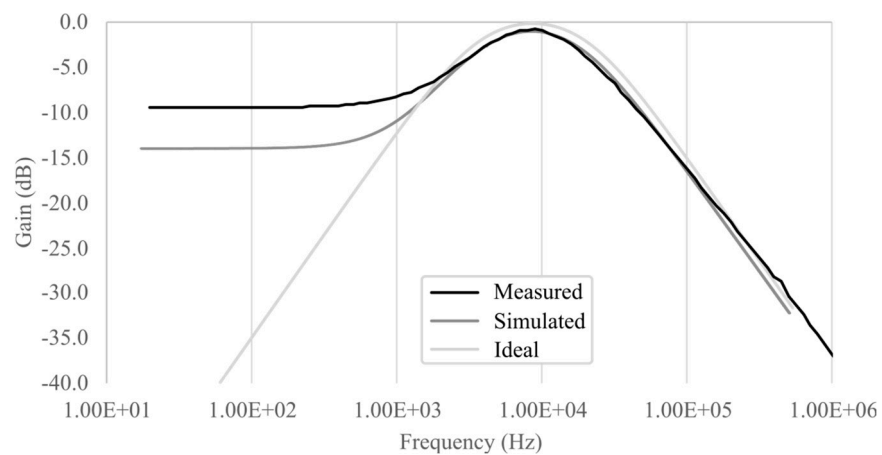
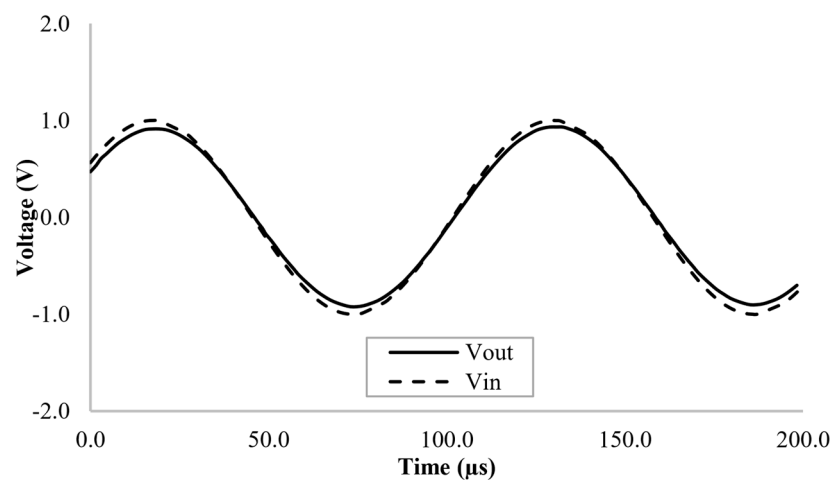


Figure 21. Experimental, simulation and ideal gain responses versus frequency.



**Figure 22.** A time-domain analysis for the band-pass filter.

As it is shown in Figures 6–8 and Figures 10–15 (SPICE simulations) as well as Figures 19, 21 and 22 (experimental verifications), the achieved time- and frequency-domain performances using the proposed SI are very close to ideal ones.

## 6. Conclusions

A new implementation for the SI based on a single  $VCII_{\pm}$  is proposed. It is composed of one  $VCII_{\pm}$  ABB, two resistors and one grounded capacitor that is attractive for IC fabrication. The prominent feature of the presented work is its low series impedance. As a result, it has the property of improved low-frequency performances. However, it is restricted with a single resistive matching condition. To test the functionality of the proposed circuit, it is used in the realization of a standard fifth-order HP ladder filter and a second-order BP filter. Simulation and experimental results approach to ideal ones but an unimportant difference arises from non-idealities of the  $VCII_{\pm}$ .

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