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Design and Implementation of High-Efficiency Converter for Direct Current Microgrid Applications

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ABSTRACT

In this study, a boost converter has been designed and implemented with high efficiency and power factor correction for microgrid applications. The designed converter consists of two main parts: the control and the power module. The control module performs functions such as reading analog data, exchanging data with other converters, operating control algorithms, and energy management among distributed generation units. On the other hand, the power module provides power transfer to the load by controlling the switching device. Also, electromagnetic interference is reduced thanks to the filters in the power module. The designed converter has a nominal power of 1000 W and provides 380 VDC output voltage regulation in the grid's input range of 85 VAC and 265 VAC. The efficiency of the proposed converter under full load is 97.02%. In addition, the converter efficiency has been tested according to European efficiency standards. The corresponding yield is measured as 95.89%. The total harmonic distortion of the input current is comfortably within limits set by the EN 6100-3-2 Class D Limits (A) standards, measuring at 1.71% when operating at full load and with a power factor of 0.998. It can be used in microgrid applications designed for high-efficiency energy management.
***Index Terms*—**Efficiency, distributed generation units, microgrid, power converter

I. INTRODUCTION

Energy production in conventional electric power systems is based mainly on fossil fuels, and this generation method has low energy efficiency. Power generation based on fossil fuels causes environmental pollution problems. In addition, another problem is the rapid depletion of fossil fuel resources used to meet the daily needs of industrialization and the increasing human population [1]. Solutions are sought for use under the microgrid (MG) roof of distributed generation units (DER) such as photovoltaic (PV) arrays, wind turbines, fuel cells, and micro-turbines. In order to maintain the quality of the energy obtained from the MG, it must be equipped with power electronics interfaces and control circuits [2, 3]. It is important to determine the parameters optimally in the converter design for efficient use of energy resources [4, 5]. Today, advanced studies are carried out to ensure power converter applications for low-cost, efficient, reliable, and easy integration.

The most critical capabilities of MGs are the management of direct current (DC) or alternating current (AC) grid types at different power levels [3], reactive power control [6], and bidirectional power flow [7, 8]. These capabilities are achieved through appropriate control techniques such as pulse width modulation (PWM) and energy management systems (EMS) based on various control algorithms [9]. Technology advancements have led to many innovations, such as the easy integration of renewable energy sources (RES) into MG. Power converters are the essential components of the RES. The energy capacities of RESs are lower than conventional energy sources, so many sources are connected in series and parallel at high power demand. Therefore, the development of DC distribution lines attracts great attention [2]. Recently, researchers have been working on DC–DC converters with high input–output ratios due to their wide application areas, such as MG integration, grid-connected converters, uninterruptible power supplies, and electric vehicle charging stations [10]. The output voltage of the DERs used in MG structures can be adapted to the desired DC bus voltage by converters [11]. Multilevel boost converters are used in an application integrating PV and fuel cell systems [12].

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Among high-gain DC–DC converters, those that are single-switch and transformerless are more widely used due to their high efficiency, low cost, and lightweight design. Similarly, controlling these converters with a single power switch under different input voltages and output power levels is simpler than using multiple switch topologies. There are many well-established studies in the literature on DC-DC converters. In their study, Qi et al. [13] proposed a single-switch and transformerless DC–DC power booster converter with a sliding-mode controller to increase DC voltage gain and reduce voltage stress on the power switch. For a specific output voltage, the converter's input voltage is regulated by controlling the conduction and switching times of the switching elements. One method of adjusting the output voltage is constant-frequency switching. In this technique, the average output voltage is controlled by adjusting the conduction time of the switches [5]. The aim of using the constant-frequency switching technique for power factor correction (PFC) is to improve the efficiency of the converter and the quality of the input current [14, 15]. More research is being conducted on switched-inductor/capacitor cell structures that enhance voltage gain by increasing the inductive and capacitive energy of the basic boost converter. [16]. In addition to these structures, quadratic cascade converters have high voltage gain without over-duty cycles [17, 18]. Tekin et al. [19] proposed a switching capacitor-based second-order boost converter structure that provides high voltage gain at low-duty cycles using a fuzzy logic controller. To validate the proposed converter's analysis and simulation results, a 200 W prototype is implemented. Similarly, various cascade converters provide high voltage gain, such as triple-lift, super-lift, etc. [20]. Furthermore, interleaved boost converters with voltage multiplier cells are converters that have both high-power ratios and high voltage gains [21]. Coupled inductor boost converters also provide high voltage gain and low switching stress at high duty ratios with high sensitivity [22, 23].

A comparison of the performance of designed converters and some other boost converters presented in the literature is given in Table I. This table includes input and output voltage, power, switching frequency, peak efficiency, voltage gain, switch voltage stress, and the number of components used in the converters. Based on this table, the gain can be increased using voltage multipliers such as switched-inductor/capacitor cells and cascaded structures in the proposed converters [16, 20–22]. However, these topologies use many components, which is a significant factor that increases the cost and size of the converters. Additionally, the presence of many components can reduce efficiency. The proposed converters in [17, 23] contain fewer components but have lower voltage gains. As the switching frequency increases in the converters, the size of components such as inductors can be reduced, leading to more compact structures. However, it also increases the switching elements' losses, negatively affecting the converter's efficiency. The proposed converter stands out among the other converters in Table I due to its high efficiency, despite having the highest switching frequency.

Due to technological advancements, the use of cascaded DC–DC converters with multiple output configurations in DC MGs has significantly contributed to DC distribution systems. However, if the parameters of the converters in a cascaded converter system are adjusted independently, it may lead to instability in the entire system. To overcome this issue, Li et al. [24] proposed a new stability analysis method in their study, which combines impedance analysis, Nyquist criterion, and identification function to accurately determine

TABLE I. PERFORMANCE COMPARISON AMONG DESIGNED CONVERTER AND SOME OTHER BOOST CONVERTERS PRESENTED IN THE LITERATURE

Ref.	V_{in} (V)	V_{out} (V)	P_{out} (W)	f_{sw} (kHz)	η (%)	Switches Numbers	Diodes Numbers	Inductors Numbers	Capacitors Numbers	Voltage Gain	Voltage Stress on Switches
[16]	12	90	40	94	≈ 91.6	1	3	1	3	$\frac{2}{1-D}$	$\frac{V_{out}}{2}$
[17]	48	150	100	20	94	1	3	2	2	$\frac{1}{(1-D)^2}$	V_{out}
[18]	20	70	24.5	50	95	2	2	2	2	$\frac{1}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$
[20]	20	660	14.5	100	78	1	8	3	6	$\left(\frac{2-D}{1-D}\right)^3$	$\frac{V_{out}}{2-D}$
[21]	20	400	400	100	94.16	2	4	2	5	$\frac{4}{1-D}$	$\frac{V_{out}}{4}$
[22]	24	400	200	50	95.31	1	6	1	6	$\frac{1+2n+nD}{1-D}$	$\frac{V_{out}}{1+2n+Dn}$
[23]	100	250	500	50	95.12	3	2	2	1	$\frac{1}{1-2D}$	V_{out}
Proposed	85-265	380	1000	200	97.02	1	1	1	1	$\frac{1}{1-D}$	V_{out}

the stability range of a cascaded DC–DC converter system. Similarly, Ahmed et al. [25] conducted an analysis and experimental study of a cascaded system consisting of a source boost converter and three load converters, including buck, cuk, and single-ended primary inductance converter.

In [26], a zero voltage switching (ZVS) boost converter is designed for use in DC MG systems. A 250 W prototype of the system has been created and verified through experimental results. Similarly, in [27], a push–pull parallel resonant converter is developed using a new control technique. Operating the proposed converter at variable duty ratios enables it to be used as both a boost and a buck converter. A 50 W prototype of the system has been implemented, and the simulation results have been experimentally validated. Another study in [28] proposes a single-input, multi-output DC converter. The proposed buck converter performs PFC with fewer switching elements than conventional rectifiers. Additionally, an experimental prototype is built to verify the proposed topology and control. In [29], a flyback converter is designed for universal input and wide load ranges. A prototype of the converter with a power rating of 48 W has been developed, and the total efficiency has been measured as 81%. In another study presented in [30], a passive damping circuit is proposed for a PFC converter, improving efficiency.

In order to ensure the balance between the supply and demand in MG, it is necessary to utilize an EMS that can track the fluctuating changes in RES. This ensures that the voltage and frequency stability of the bus is kept within certain operating limits. Awaad and Afifi [31] have designed, simulated and implemented a DC MG based on a quadrupler boost converter. The proposed converter is controlled using an adaptive droop technique to achieve proper load sharing. In [32], an improved virtual capacitor parallel coordination control strategy based on a multi-port isolated DC–DC converter topology is proposed to improve the DC bus voltage quality and overcome the balancing problem of energy storage systems in MGs. In MG, DERs such as PV arrays, wind turbines, and diesel generators are utilized, and these sources are connected to the load through a converter. When AC DERs are used in DC MGs, their outputs must be rectified. However, it should be noted that high harmonic distortion occurs during this rectification process. Additionally, when there is a phase difference between voltage and current, the actual power delivered to the load is reduced. Therefore, a PFC function should be added to bring the power factor closer to 1 and to reduce the total harmonic distortion.

The aim of this study is to design a high-efficiency converter with a PFC function to minimize the total harmonic distortion of source currents and the phase difference between current and voltage in MG applications. The boost converter covers a wide voltage range between 85 VAC and 265 VAC. The output voltage regulation of 380 VDC is achieved by the control module operated by the controller. The proposed converter has a power output of 1000 W, and experimental tests have been carried out in accordance with European efficiency standards. The control module of the converter utilizes an STM32F407VG6T microcontroller with ARM architecture. The CAN communication unit on the designed control module aims to provide stable and balanced energy management by enabling the DER units to communicate with each other for electrical quantities such as current, voltage, and power. Additionally, the UART communication unit on the module is designed to enable all data of the DER units to be stored in a computer environment.

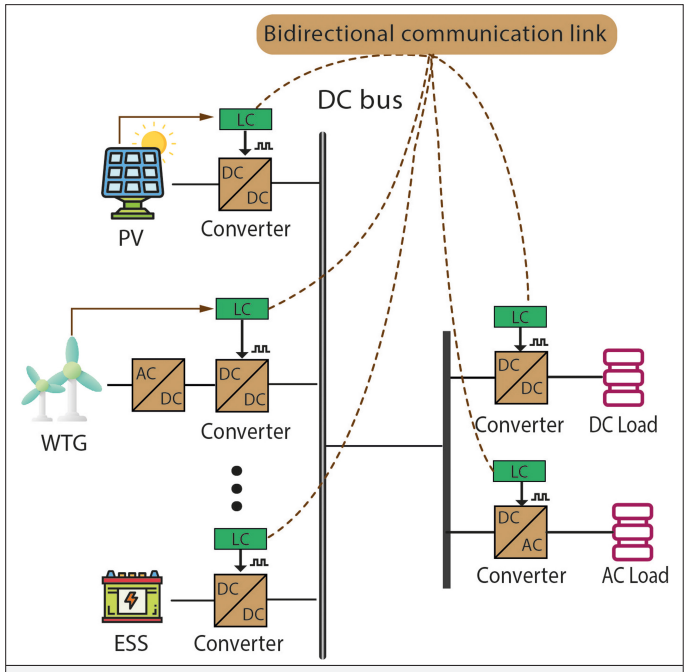

Fig. 1. Typical configuration of direct current microgrid.

II. DESIGN OF BOOST CONVERTER

Microgrids can be defined as distributed generation grids that operate in grid-connected and/or island modes, using many modern power technologies such as DERs and energy storage units. A typical MG may include PV arrays, wind turbines, energy storage systems, DC/DC and DC/AC power converters, and local loads. The configuration of a basic DC MG is given in Fig. 1.

The aim of this study is to design a high-efficiency converter for use in DC MGs. The converter's output voltage constitutes the MG's DC bus voltage. An electromagnetic interference (EMI) filter and a bridge rectifier are added to the input of the converter, allowing energy obtained from both AC and DC sources of DER to be transferred to the DC bus via the designed converter. In this section, the design parameters of the presented converter are detailed. The basic circuit elements used in the converter are calculated according to the following specifications: the output power of the prototype design is $P_{out} = 1000\,W$, the DC bus voltage level is $V_{out} = 380\,V$, the effective value of the input voltage is $V_{in} = 85 - 265\,VAC$, and the switching frequency is $f_{sw} = 200\,kHz$.

A. Design and Determination of Parameters

The boost converter has advantages such as a simple circuit design and low cost due to its structure [33]. The equivalent circuit diagram of the converter addressed in this study is given in Fig. 2. In the boost converter topology, the V_{out} output voltage is always greater than the V_{in} input voltage in steady-state operation. The boost inductor L_1, bridge diode D_1, boost diode D_2, controllable semiconductor switch S, input filter capacitor C_{in}, output filter capacitor C_{out}, and load resistor R_L represent the converter's fixed components.

Parameters such as the inductance value, minimum input voltage, maximum duty cycle, amount of current ripple in the inductor, and output power affect the inductor value of the converter. Accordingly,

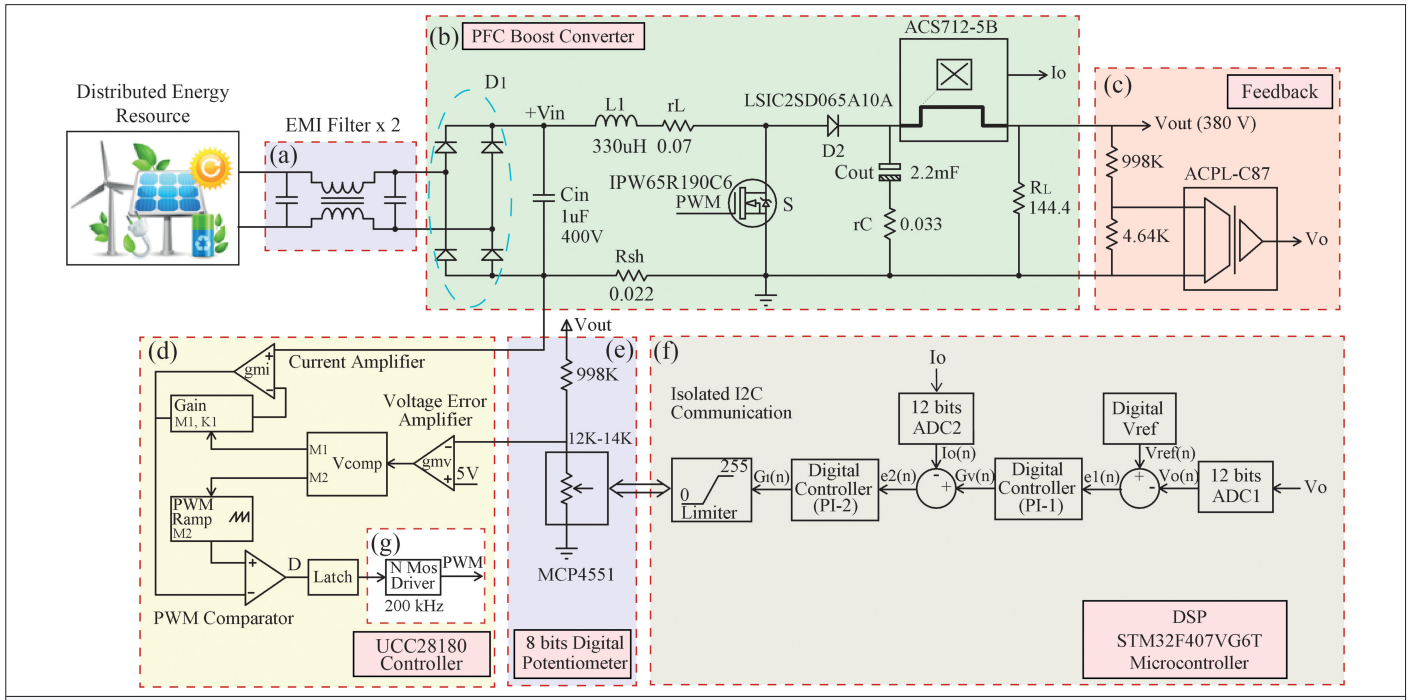

Fig. 2. The principle equivalent circuit diagram of the converter includes (a) EMI filter, (b) PFC boost converter, (c) feedback circuit, (d) UCC28180 controller, (e) digital potentiometer, (f) STM32F407VG6T microcontroller, and (g) MOSFET driver. PFC, power factor correction.

the inductance of the converter's inductor is calculated using (1)–(5). Additionally, the assumption that the average inductor current cannot exceed 20% for all operating conditions has been taken into account in the variation of the inductor current [34].

$$V_{rect.in(min)} = \sqrt{2}V_{in(min)} \tag{1}$$

$$D_{max} = \frac{V_{out} - V_{rect.in(min)}}{V_{out}} \tag{2}$$

$$I_{in(max)} = \frac{\sqrt{2}P_{out}}{\eta V_{in(min)} PF} \tag{3}$$

$$I_{rp} = \Delta I_{rp} I_{in(max)} \tag{4}$$

$$L_1 \geq \frac{V_{rect.in(min)} D_{max}}{I_{rp} f_{sw}} \tag{5}$$

Here, $V_{rect.in(min)}$ represents the minimum value of the rectified input voltage, $V_{in(min)}$ represents the minimum value of the input voltage, D_{max} represents the maximum duty cycle, $I_{in(max)}$ represents the maximum input current, η represents the converter efficiency, PF represents the power factor, I_{rp} represents the ripple current of the inductor, and ΔI_{rp} represents the ripple current ratio. An ETD 44/22/15-N87 core has been used in the ferrite core of the boost inductor. The ferrite core is wound with 48 turns, and a 1.3 mm air gap is left. The output voltage ripple is limited to 1% for all operating conditions. Accordingly, the value of the output capacitor is obtained using (6) [35].

$$C_o \geq \frac{P_{out}}{2\pi \cdot f_{line} \cdot \Delta V_{out} \cdot V_{out}} \tag{6}$$

Here, f_{line} represents the operating frequency of the DER unit, and ΔV_{out} represents the voltage ripple at the output. According to the equations earlier, L_1 and C_{out} is selected as 330 uH and 2.2 mF, respectively, for continuous conduction mode operation. Kendeil's 390 µF/450 V capacitors are chosen for the converter, with an equivalent series resistance (ESR) value of 0.2 Ω. The six capacitors are connected in parallel to achieve the calculated capacitance value, resulting in a lower power loss due to the ESR value of the capacitors decreasing to 0.033 Ω. The values of the selected and calculated design parameters for the designed boost converter are given in Table II.

TABLE II. DESIGN PARAMETERS AND VALUES FOR THE BOOST CONVERTER

Description	Symbol	Value
Nominal power	P_{out}	
Input voltage range	V_{in}	$85-265\,V_{rms}$
Nominal input voltage (AC)	$V_{in,nom}$	$230\,V_{rms}$
Nominal output voltage (DC)	V_{out}	$380\,V$
Maximum output voltage ripple	ΔV_{out}	$3.8\,V\,(\%1)$
Maximum inductor current ripple rate	ΔI_{rp}	0.2 (%20)
The inductance value of the inductor	L_1	$330\,\mu H$
The capacitance of the output capacitor	C_{out}	$2.2\,mF$
Switching frequency	f_{sw}	$200\,kHz$

B. Closed-Loop Control Strategy

A closed-loop control system is a control system that continuously measures the performance of a system through a feedback mechanism and ensures that it reaches the desired values by taking corrective actions when necessary. Such a control system should respond quickly to changes in the design, providing stable performance. The transfer function of the system is used for closed-loop control. First, mathematical equations that define the system dynamics are obtained. These mathematical equations are called constant coefficient differential equations for linear or linearized systems. The system's transfer function is obtained by taking Laplace transforms of these equations under zero initial conditions.

The UCC28180 internal controller and STM32F407VG6T microcontroller are used for the control of the converter. To obtain the general transfer function of the system, first, the transfer function of UCC28180 is obtained. For this purpose, as shown in Fig. 2(d), the internal loop factors M1 and M2 are obtained using the internal controller constants K1 and KFQ. The product of M1 and M2 is determined, and the open loop is compensated. The current loop gain factor M1, voltage loop PWM slope M2, and nonlinear gain variable M3 are obtained using (7)–(10) [34].

$$M_1 = 0.313V_{comp} - 0.401 = 0.3815 \tag{7}$$

$$M_2 = \frac{f_{sw}}{65kHz}0.1223\left(V_{comp} - 0.5\right)^2 = 1.5052\frac{V}{\mu s} \tag{8}$$

$$M_3 = \frac{f_{sw}}{65kHz}\frac{V}{\mu s}0.1148{V_{comp}}^2 - 0.1746V_{comp} + 0.0586 = 1.0449\frac{V}{\mu s} \tag{9}$$

$$M_1M_2 = 0.3815*1.5052\frac{V}{\mu s} = 0.5742\frac{V}{\mu s} \tag{10}$$

V_{comp} is the compensation voltage value obtained from the UCC28180 datasheet. This value is obtained as 2.5 V at full load and nominal operating voltage. In order to obtain the voltage transfer function, the gains of the voltage feedback (G_{FB}), pulse width modulator (G_{PWM}), and voltage error amplifier (G_{EA}) must be calculated. G_{FB} is obtained from the feedback circuit at the converter's output and is calculated according to (11).

$$G_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} = \frac{13.3K'}{998K' + 13.3K'} = 0.0132 \tag{11}$$

Here, R_{FB1} and R_{FB2} are the resistors in the feedback circuit. The transfer function of G_{PWM} is calculated according to (12)–(13).

$$f_{PWM} = \frac{M_1M_2V_{in(nom)}^2K_{FQ}}{2\pi K_1\,2.5R_{sh}V_{out}^3C_{out}} = 1.1443\,Hz \tag{12}$$

$$G_{PWM} = \frac{\dfrac{M_3V_{out}}{M_1M_2\blacklozenge 1V}}{1 + \dfrac{s}{2\pi f_{PWM}}} = \frac{5000}{s + 7.19} \tag{13}$$

The characteristic frequency of the PWM signal is denoted by f_{PWM}, and $K_1 = 7$ and $K_{FQ} = 1/f_{sw}$ represent the internal controller constants. The transfer function of G_{EA} is obtained from (14).

$$G_{EA} = g_{mv}\left[\frac{1 + sR_{VCOMP}C_{VCOMP}}{\left(C_{VCOMP} + C_{VCOMP\_P}\right)s\left[1 + s\left(\dfrac{R_{VCOMP}C_{VCOMP}C_{VCOMP\_P}}{C_{VCOMP} + C_{VCOMP\_P}}\right)\right]}\right] \tag{14}$$

$$= \frac{7.789\cdot 10^{-6}s + 5.6\cdot 10^{-5}}{8.286\cdot 10^{-8}s^2 + 1.041\cdot 10^{-5}s}$$

In this Equation, $g_{mv} = 56\,\mu S$ represents the transconductance gain, and R_{VCOMP}, C_{VCOMP}, and C_{VCOMP_P} represent the compensation components. These components are calculated based on the specified parameters in the UCC28180 control integrated circuit's datasheet, resulting in values of 14.2 KΩ, 10 μF, and 0.56 μF, respectively. Taking all of these values into account, the closed-loop transfer function of the controller, G_{VL}, is expressed in (15).

$$G_{VL} = G_{FB}\cdot G_{PWM}\cdot G_{EA} = \frac{3.3864\cdot 10^{-4}s + 2.2778\cdot 10^{-3}}{8.286\cdot 10^{-8}s^3 + 1.101\cdot 10^{-5}s^2 + 7.486\cdot 10^{-5}s} \tag{15}$$

In Fig. 3, Bode magnitude and phase plots of the closed-loop transfer function G_{VL} are presented. According to the plot, the magnitude value at low frequencies for $G_{VL}\left(j\omega\right)$ is obtained as $20log\left|G_{VL}\left(j0\right)\right| = 71.4\,dB$. As the frequency increases, the magnitude continues to decrease with the effect of the zero at $= -7.1894$ $\left(\omega = 7.1894\,rad/s\ or\ f_{PWM} = 1.1443\,Hz\right)$. A pole is placed at $s = -125.6866\left(f_{pole} = 20\,Hz\right)$ to reject high-frequency noise and roll off the gain amplitude.

The reference voltage of the UCC28180 internal controller is implemented in the microcontroller section. This reference voltage is determined by the cascade proportional integral derivative (PID) controller inside the microcontroller. The transfer function and closed-loop control model of the designed converter are given in Fig. 4. The designed controller should maintain the 380 V output voltage under variable disturbances in order to provide the requested power and ensure stable voltage regulation.

The PID controller parameters for the PFC boost converter are obtained using the Ziegler–Nichols method based on the feedback closed-loop transfer function [36, 37]. In the Ziegler–Nichols method, the integral time constant is set to infinity and the derivative time constant is set to 0, effectively disabling the integral and derivative actions. By doing so, the oscillation period is determined based on the maximum oscillation within the stability boundary, and the proportional, integral, and derivative gains are then determined accordingly. The step responses of the cascaded proportional integral (PI), proportional derivative (PD), and PID controllers, based on the closed-loop transfer function of the designed converter, are compared in Fig. 5.

The PD controller provides the controller with anticipation against the increasing or decreasing trend of the error signal by adding the derivative of the error signal to the control signal. This way, the control system gains the ability to follow rapid changes. When the performance of the PD controller, which is obtained by unit step response in Fig. 5 and Table III, is examined among the other controllers, it is seen that it gives the best results with a rise time of 0.059 s and a settling time of 0.220 s. However, it has been observed that the closed-loop PD controller used in experimental studies caused a steady-state error in the control signal when

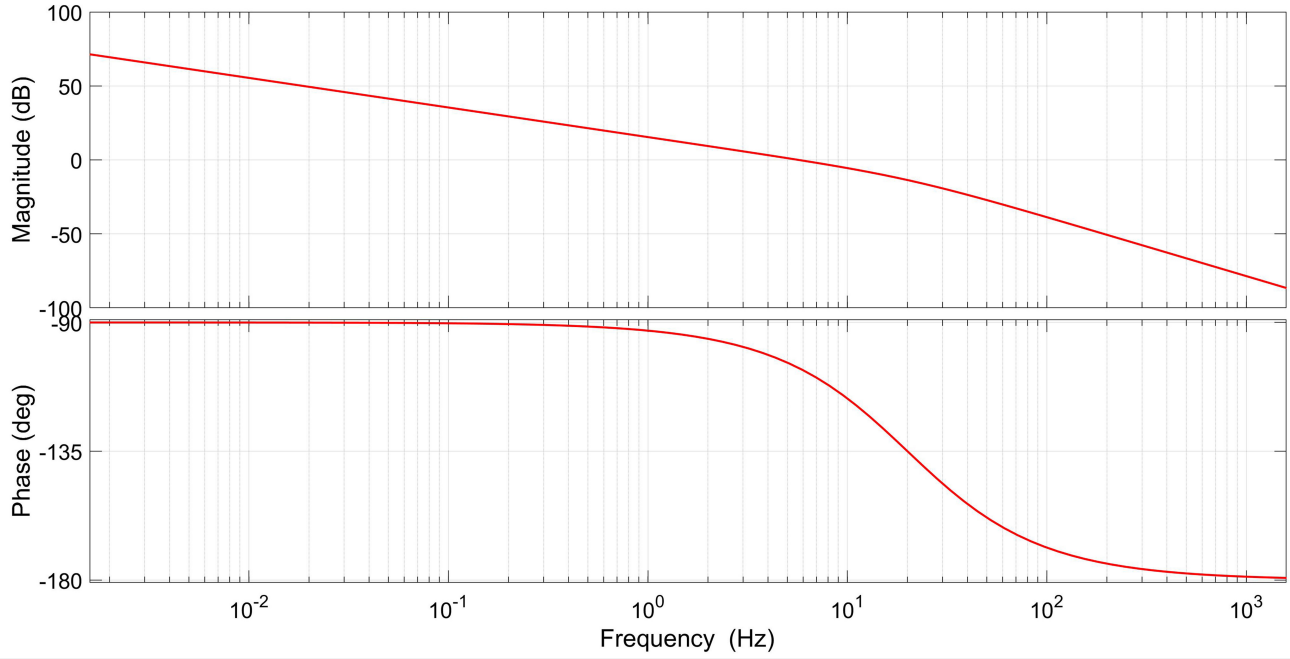

Fig. 3. Bode magnitude and phase curves of closed-loop transfer function G_{VL}.

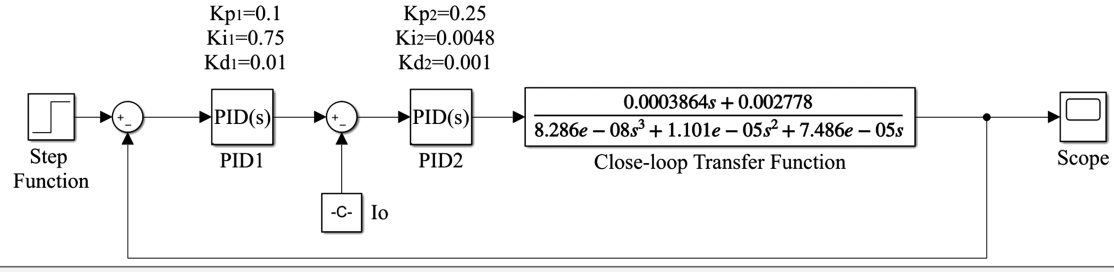

Fig. 4. Transfer function and closed-loop control model of the designed converter.

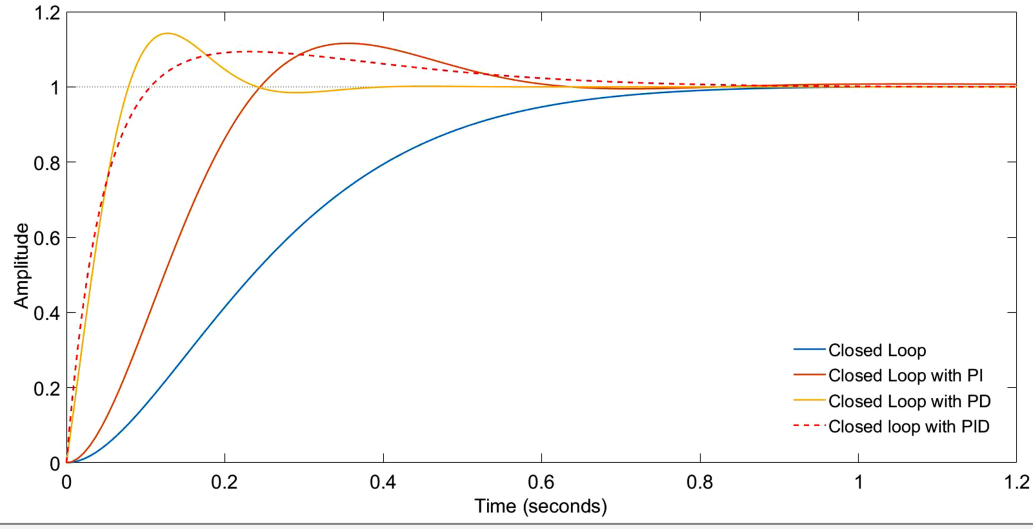

Fig. 5. Response of PI, PD and PID controllers to step response.

TABLE III. PERFORMANCE ANALYSIS OF CONTROL METHODS

Parameters	Closed Loop (CL)	CL with PI	CL with PD	CL with PID
Rise time (s)	0.436	0.165	0.059	0.072
Settling time (s)	0.721	0.562	0.220	0.625
Overshoot (%)	0.623	11.5884	14.2566	9.3735

exposed to a disturbance input. Therefore, a PID controller is preferred for the converter control designed for MG structures. Thus, a steady-state error is eliminated with the integral term, and the ability to adapt to fast-changing conditions is provided through the derivative term. Additionally, using a PID controller resulted in the best performance among other controller types, with an overshoot of 9.37%.

In this study, the optimal proportional coefficients for cascade PID controllers were determined as $K_{p1}=0.1$, $K_{p2}=0.25$, integral coefficients as $K_{i1}=0.75$, $K_{i2}=0.0048$, and derivative coefficients as $K_{d1}=0.01$, $K_{d2}=0.001$.

C. Selection of Semiconductor Equipment and Efficiency Calculations

The efficiency of converters is an indicator of how little energy is lost during the energy conversion process. Effective methods such as high-efficiency components, optimized converter topologies, ZVS and zero current switching techniques, and temperature control of components are used to increase the efficiency of converters. Parameters of switching elements such as MOSFETs have a significant impact on the performance and efficiency of converters. As the internal resistance, capacitive effects, switching speeds, maximum current-voltage values, temperature coefficients, and noise levels of these switching elements affect the efficiency of converters, it is important to select and optimize the correct parameters during the design phase.

D25XB60 bridge-type rectifier is preferred in the designed converter. The catalog data of the rectifier are given in Table IV. The average input current of the diode (I_{D1}) is calculated according to (16), and the switching power loss (P_{D1}) is calculated according to (17) [35].

$$I_{D1}=\frac{2}{\pi}\cdot\frac{\sqrt{2}\cdot P_{out}}{V_{in}}=3.91\,A \tag{16}$$

$$P_{D1}=2\cdot I_{D1}\cdot V_F=8.22W \tag{17}$$

Here V_F is the diode's maximum forward voltage. P_{D1} is calculated as 8.22 W.

Infineon's IPW65R190C6 is preferred as a switching device because of low internal resistance and shorter length of the miller plateau

TABLE IV. TECHNICAL SPECIFICATIONS OF THE D25XB60

Maximum Peak Reverse Voltage	Maximum RMS Voltage	Maximum Forward Voltage per Diode	Maximum Average Forward Current
600 V	420 V	1.05 V	25 A

TABLE V. TECHNICAL SPECIFICATIONS OF THE IPW65R190C6

$V_{DS,max}$	$I_{D,max}\,(25°C)$	R_{dson}	C_{rss}	C_{iss}	Q_g	E_{oss}
700 V	20.2 A	0.190 Ω	100 pF	1620 pF	73 nC	5.9 µJ

characteristics. The data containing the characteristic features of this switching element are provided in Table V. The current flowing through the drain-source pins of the MOSFET ($I_{s,rms}$) is obtained using (18), and the dynamic loss of the MOSFET ($P_{s,cond}$) is obtained using (19).

$$I_{s,rms}=\frac{P_{out}}{V_{in}}\sqrt{1-\frac{8\sqrt{2}\cdot V_{in}}{3\cdot\pi\cdot V_{out}}}=2.27A \tag{18}$$

$$P_{s,cond}=I_{s,rms}{}^2\cdot R_{dson}=0.98\,W \tag{19}$$

Here, R_{dson} represents the on-state internal resistance of the MOSFET. $P_{s,cond}$ is calculated as 0.98 W. Similarly, the turn-on time (t_{on}) of the MOSFET is calculated using (20). The turn-on switching power loss ($P_{s,on}$) is calculated by (21) [35].

$$t_{on}=C_{iss}\cdot R_g\cdot In\left(\frac{V_g-V_{th}}{V_g-V_{pl}}\right)+C_{rss}\cdot R_g\left(\frac{V_{ds}-V_{pl}}{V_g-V_{pl}}\right)=9.35\,ns \tag{20}$$

$$P_{s,on}=0.5\cdot I_{L,rms}\cdot V_{out}\cdot t_{on}\cdot f_{sw}=1.05W \tag{21}$$

Here C_{iss} is the input capacitance value of the MOSFET, $R_g=2\,\Omega$ is the gate resistance, $V_g=15\,V$ is the gate voltage, $V_{th}=3.5\,V$ is the gate threshold voltage, $V_{pl}=5.5\,V$ is the gate plateau voltage, C_{rss} is the gate-drain capacitance, V_{ds} is the drain-source voltage, and $I_{L,rms}$ is the effective value of the inductor current. Similarly, the turn-off time (t_{off}) is calculated by (22), and the turn-off switching power loss ($P_{s,off}$) is calculated by (23).

$$t_{off}=C_{rss}\cdot R_g\left(\frac{V_{ds}-V_{pl}}{V_{pl}}\right)+C_{iss}\cdot R_g\cdot In\left(\frac{V_{pl}}{V_{th}}\right)=16.59ns \tag{22}$$

$$P_{s,off}=0.5\cdot I_{L,rms}\cdot V_{out}\cdot t_{off}\cdot f_{sw}=1.87W \tag{23}$$

$P_{s,on}$ and $P_{s,off}$ are calculated as 1.05 W and 1.87 W, respectively. The output capacitance switching loss ($P_{s,oss}$) and gate drive loss ($P_{s,gate}$) are obtained by (24) and (25), respectively.

$$P_{s,oss}=E_{oss}\cdot f_{sw}=1.18W \tag{24}$$

$$P_{s,gate}=V_g\cdot Q_g\cdot f_{sw}=0.22W \tag{25}$$

Here, Q_g is the gate charge total, and E_{oss} is the amount of energy required to charge the MOSFET's output capacitance. $P_{s,oss}$ and $P_{s,gate}$ are calculated as 1.18W and 0.22W, respectively. Accordingly, the total power loss (P_S) in the MOSFET is calculated by (26) as 5.30 W.

$$P_S=P_{s,cond}+P_{s,on}+P_{s,off}+P_{s,oss}+P_{s,gate}=5.30\,W \tag{26}$$

LSIC2SD065A10A boost diode is preferred due to its low capacitive charge characteristic. The boost diode conduction loss ($P_{D,cond}$),

switching loss ($P_{D,switch}$), and boost diode total loss (P_{D2}) are calculated by (27)–(29). The data containing the characteristics of the boost diode are given in Table VI.

$$P_{D,cond} = \frac{P_{out}}{V_{out}} \cdot V_{Fb} = 3.95W \quad (27)$$

$$P_{D,switch} = 0.5 \cdot V_{out} \cdot Q_c \cdot f_{sw} = 1.14 \cdot \mathrm{W} \quad (28)$$

$$P_{D2} = P_{D,cond} + P_{D,switch} = 5.09\,\mathrm{W} \quad (29)$$

Here Q_c is the total capacitive charge value of the diode and V_{Fb} is the boost diode's forward voltage. P_{D2} is calculated as 5.09 W. Similarly, capacitor effective current $(I_{Co,rms})$ and capacitor ESR loss (P_{Co}) are calculated by (30) and (31), respectively. P_{Co} is calculated as 0.23 W.

$$I_{Co,rms} = \sqrt{\frac{8 \cdot \sqrt{2} \cdot P_{out}^2}{3 \cdot \pi \cdot V_i \cdot V_{out}} - \frac{P_{out}^2}{V_{out}^2}} = 2.61A \quad (30)$$

$$P_{Co} = I_{Co,rms}^2 \cdot ESR = 0.23W \quad (31)$$

The total loss in the inductor consists of copper and core loss. The effective value of the inductor's current (I_{Lrms}) and the copper loss (P_{Cl}) is calculated by (32) and (33), respectively.

$$I_{Lrms} \cong I_{in,rms} = \frac{P_{out}}{V_{in,nom}} = 4.35\ A \quad (32)$$

$$P_{Cl} = I_{Lrms}{}^2 .DCR = 1.32W \quad (33)$$

Here, DCR is the DC resistance constituted by wrapping 48 turns of 1.12 mm diameter wire. Accordingly, P_{Ll} is calculated as 1.32 W. The inductor core loss (P_{core}) is calculated by (34).

$$P_{core} = P_v \cdot V_e = 8.20\,\mathrm{W} \quad (34)$$

Here P_v represents the power loss at 200 kHz switching frequency, 100 mT peak magnetic flux density and 40°C temperature value, and its value 230 kW/m^3. V_e is the core volume, and its value is $2 \times 17819 \times 10^{-9}$ m^3. P_{core} is calculated as 8.20 W. So the total power loss (P_{loss}) of the converter and the converter efficiency $(\%\eta)$ are calculated by (35) and (36), respectively [13].

$$P_{loss} = P_{core} + P_{Cl} + P_{D1} + P_{D2} + P_{Co} + P_S = 28.36\,W \quad (35)$$

$$\eta = \frac{P_o}{P_o + P_{loss}} = \frac{1}{1 + \frac{P_{loss}}{P_{out}}} = 97.24\% \quad (36)$$

As a result of theoretical calculations, the converter's P_{loss} is calculated at 28.36 W, and theoretical efficiency at full load is calculated as 97.24%. The power losses in the designed converter are given in Fig. 6.

D. Design of the Printed Circuit Board and Mounted

The converter consists of two parts: the control and the power module. In this way, it is aimed to reduce electromagnetic interference and facilitate fault detection. The three-dimensional (3D) schematic preview of the control module is given in Fig. 7. Isolation chips are used on the control module, thus providing isolation between the microcontroller and the peripherals. Thus, electromagnetic interferences and switching noises in voltage and current data, read by the analog-digital converter unit of the microcontroller, are minimized.

The 3D schematic preview of the power module is given in Fig. 8. ACS712-05B hall effect sensor is used to read current. IS341W device is preferred for the MOSFET gate drive circuit. Both devices have an isolated circuit. Thus, isolation is provided in the power module as well as in the control module. The flyback converter provides the energy requirement of the control and power module. Filter designs have been carried out to minimize electromagnetic interference in both the boost and the flyback converter.

III. IMPLEMENTATION AND EXPERIMENTAL RESULTS

In this study, a high-efficiency boost power converter with a PFC process is designed for MG applications. The converter's power is 1000 W, and the switching frequency is 200 kHz. The converter's real-time application is implemented to verify the designs and make objective observations experimentally. The experimental setup of the boost converter is given in Fig. 9. The prototype converter's experimental test results under the different conditions are listed in Table VII. The efficiency analysis of the designed converter is measured according to European testing standards.

When examining the experimental results presented in Table VII, it can be observed that the converter achieves an efficiency of 96.83% at half load and 97.02% at full load. The efficiency results obtained from theoretical calculations and experimental measurements, depending on the output power, are illustrated in Fig. 10. As seen

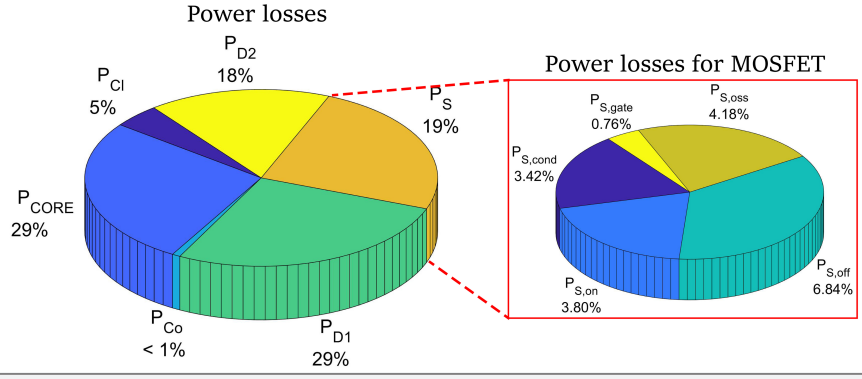

Fig. 6. Total power losses in the components of the prototype converter.

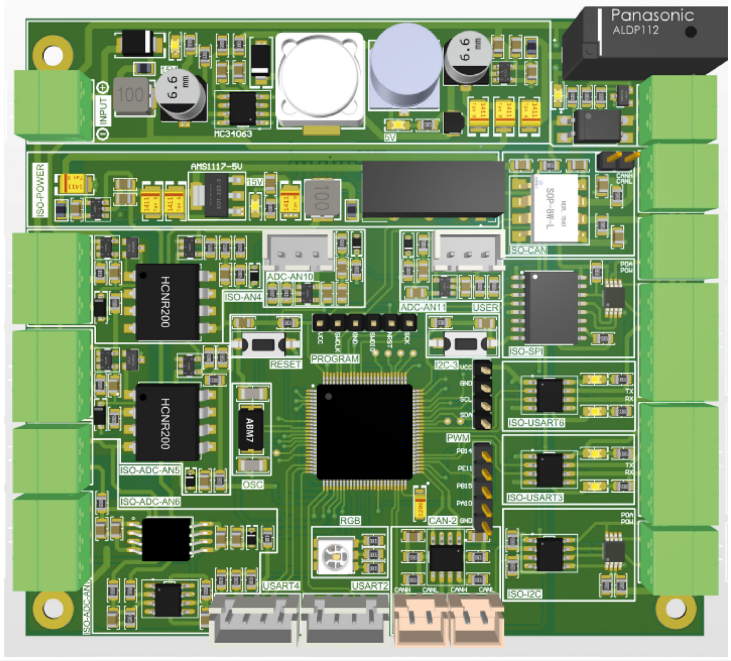

Fig. 7. Three-dimensional preview of the control module.

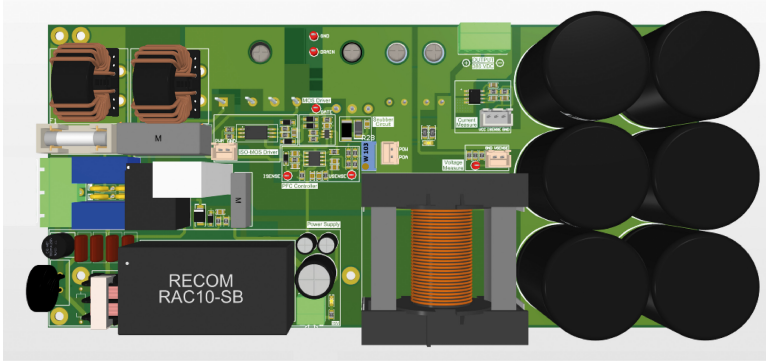

Fig. 8. Three-dimensional preview of the power module.

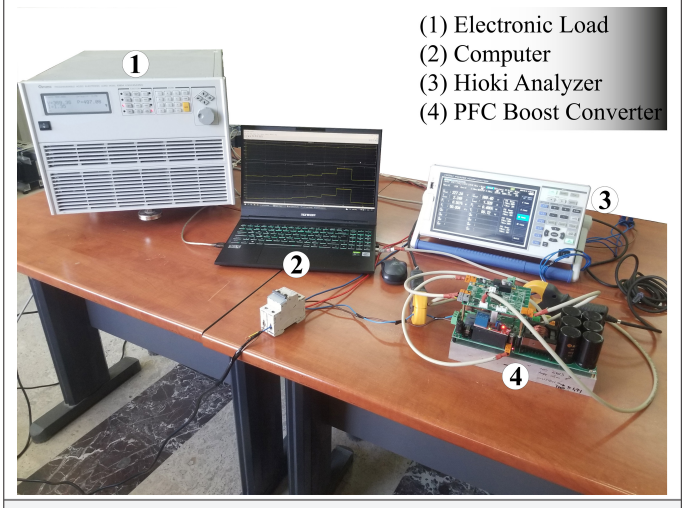

Fig. 9. The converter's experimental setup.

from this figure, the experimental results agree with the theoretical calculations and confirm the design of the converter. For instance, while the calculated efficiency at full load is 97.24%, the measured efficiency is 97.02%.

The converter's efficiency is obtained according to the European efficiency standards using (37) [38]. Accordingly, the EU-weighted efficiency of the designed converter is calculated as 95.89% according to European efficiency standards.

$$EU_{\eta} = 0.03\eta_{5\%} + 0.06\eta_{10\%} + 0.13\eta_{20\%} + 0.1\eta_{30\%} + 0.48\eta_{50\%} + 0.2\eta_{100\%} = 95.89 \quad (37)$$

TABLE VI. TECHNICAL SPECIFICATIONS OF THE LSIC2SD065A10A

DC Blocking Voltage	Continuous Forward Current	Forward Voltage	Total Capacitive Charge
650 V	27 A	1.5 V	30 nC

TABLE VII. EXPERIMENTAL TEST RESULTS VERSUS INPUT AND OUTPUT OF THE POWER FACTOR CORRECTION BOOST CONVERTER

Input Values			Output Values						Efficiency (%)	
$V_{in,rms}$ (V)	$I_{in,rms}$ (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	PF	THD (%)	Total Power Loss (W)	Calculated	Measured
228.48	0.348	57	380.41	0.129	49	0.959	6.25	8	87.01	86.52
228.17	0.521	107	381.38	0.260	99	0.963	5.76	8	91.56	91.41
227.78	0.957	210	379.86	0.527	200	0.981	5.15	10	94.30	94.81
227.66	1.401	313	379.52	0.793	301	0.986	4.62	12	95.46	96.03
227.43	2.290	517	379.57	1.320	501	0.995	2.81	16	96.49	96.83
226.01	4.601	1038	380.10	2.649	1007	0.998	1.71	31	97.24	97.02

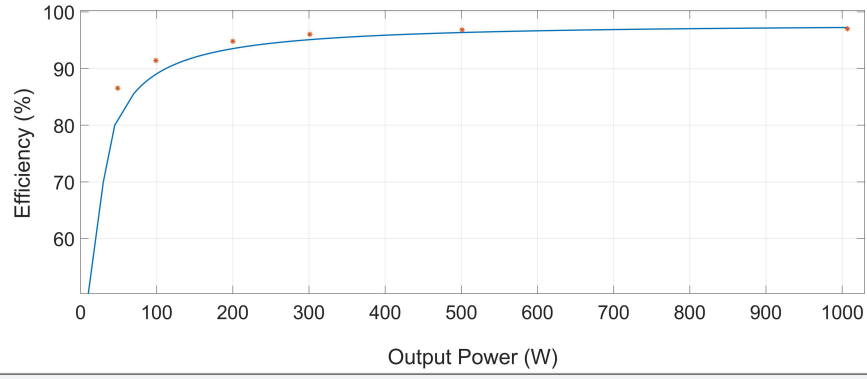

Fig. 10. Efficiency calculated and measured under different load conditions according to European standards.

The performance of the proposed converter has been tested under six different load conditions given in European efficiency standards. The output characteristic of the converter under variable load conditions is observed in Fig. 11. It is seen that the proposed converter has a robust controller characteristic and restores the output voltage at 380 V under both transient and steady-state conditions.

Furthermore, the performance of the proposed converter has been investigated for varying input voltages. The test results for

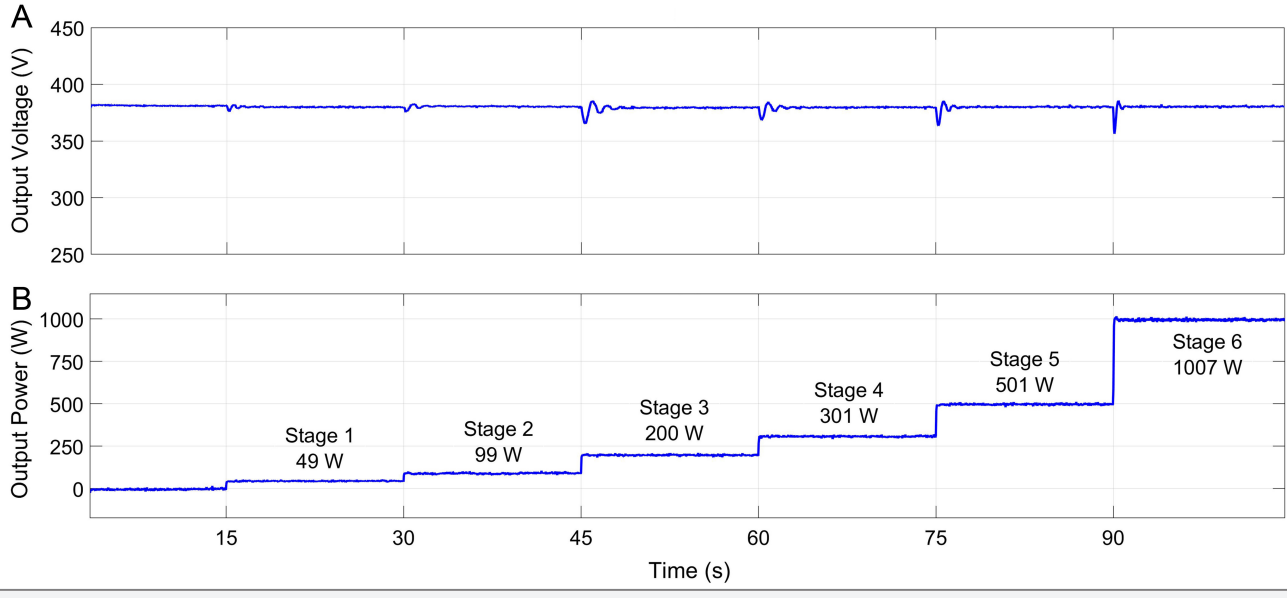

Fig. 11. The test results of the proposed converter according to European efficiency standards: (a) output voltage and (b) output power.

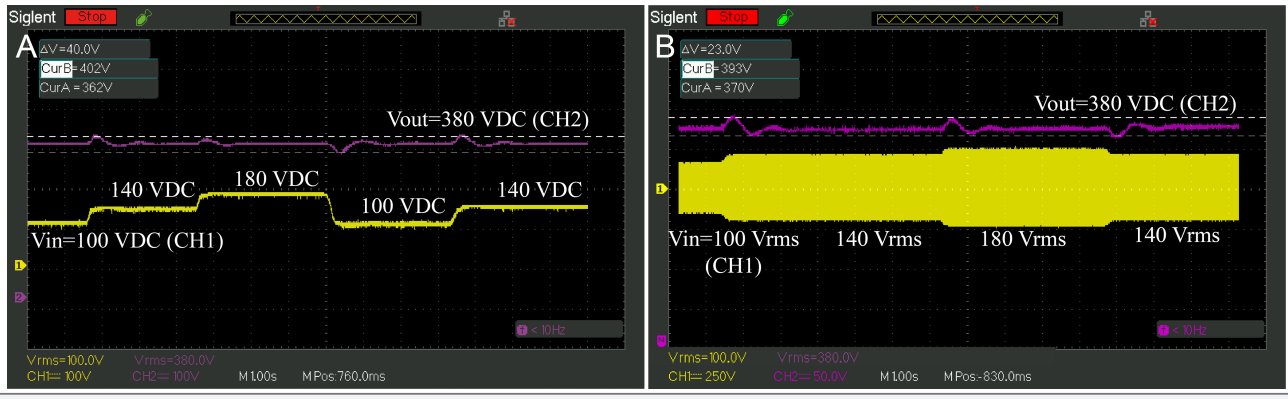

Fig. 12. The performance of the proposed converter under different input voltages (CH1 input, CH2 output). (a) DC input and (b) AC input.

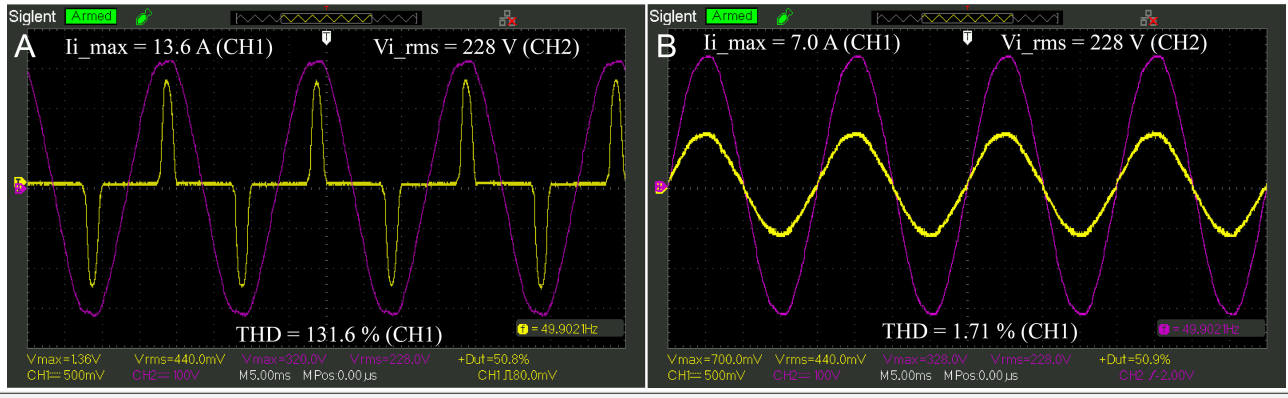

Fig. 13. Input current (CH1) and input voltage (CH2) graphs of the converter at full load (a) without PFC (b) with PFC. PFC, power factor correction.

output voltage against different DC input voltages are presented in Fig. 12(a), and for different AC input voltages in Fig. 12(b). As clearly seen from the figures, the designed converter restores the output voltage at a stable 380 V value under both DC and AC input voltages.

The current and voltage characteristics under full load are analyzed for PFC and non-PFC conditions, as shown in Fig. 13(a) and (b). Both experiments are carried out under the same conditions with an input power of 1003 W and an input voltage of 228 V RMS. Without PFC, the maximum input current reaches 13.6 A with a total harmonic distortion of 131.6%. In contrast, with PFC activated, the maximum input current and total harmonic distortion are reduced to 7 A and 1.71%, respectively. The results clearly demonstrate a 48.53% reduction in the maximum input current and a 98.70% improvement in harmonic distortion achieved by the activation of PFC.

It was assumed that the output voltage ripple would not be more than 1% in the design progress. The output voltage and its ripple when the converter is at full load are given in Fig. 14. The output voltage is 380 V, and the maximum peak voltage is 384 V. The ripple is detected as 1.05%. This value corresponds to the voltage ripple limit value specified in the design. Accordingly, the experimental results confirm the design parameters.

The MOSFET's turn-on and turn-off times can cause switching noises in the converter's output voltage. To reduce the peak voltage stress

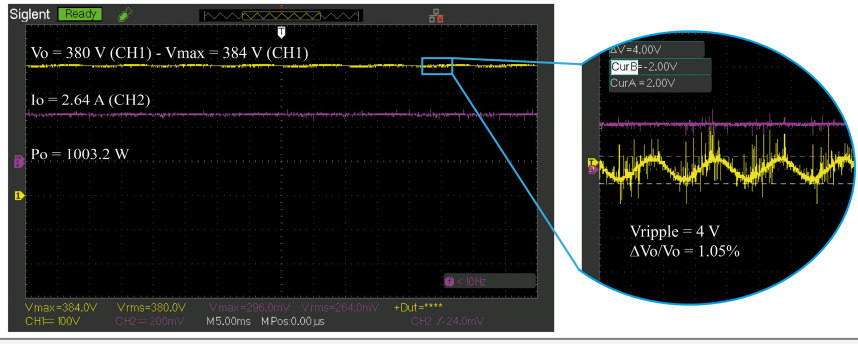

Fig. 14. Output voltage (CH1) and output current (CH2) graphs when the converter is at full load.

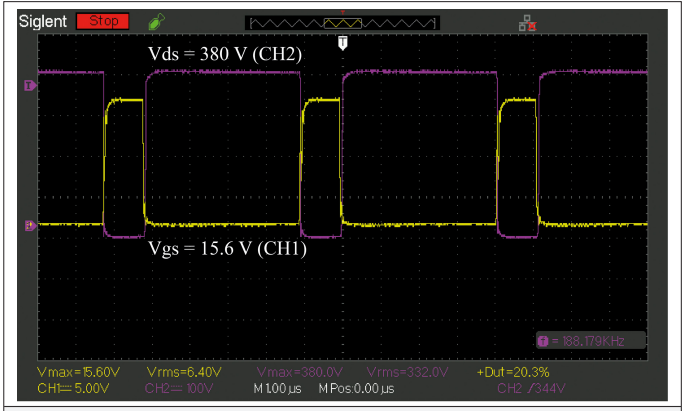

Fig. 15. PWM signals at the gate and drain terminals of the MOSFET; V_{gs} voltage (CH1) and V_{ds} voltage (CH2). PWM, pulse width modulation.

between the MOSFET's drain-source terminals, a R_{gate} resistor is added to the gate terminal. In this study, the value of R_{gate} is determined as 2 Ω to minimize the voltage stress on the MOSFET. Fig. 15 illustrates the signals between the gate-source and drain-source terminals of the MOSFET in this situation. As depicted in the figure, the switching MOSFET's voltage stress is significantly reduced.

IV. CONCLUSION

The power electronics-based equipment used in MGs are converters that regulate the voltage between DERs and the DC bus. They are also necessary to manage energy between loads and DERs. In this study, a PFC boost converter has been designed and experimentally verified for DC MG applications. The designed converter has been made suitable for use in AC DERs by adding a full wave rectifier circuit and filters to its input. Thus, it can be used for both DC and AC output DERs. The PFC boost converter designed has a 1000 W output power, 85–265 Vrms AC input, 380 V DC output, and a 200 kHz switching frequency. The converter has high efficiency, with a full load efficiency of 97.02%.

Furthermore, the converter has been tested according to European efficiency standards, and the efficiency measured is 95.89%. The total harmonic distortion of the input current (THDi) is well below the EN 6100-3-2 Class D Limits (A) standards, with a THDi of 1.71% and a power factor of 0.998 measured at full load. Consequently, the converter can be used for both AC and DC DERs in DC MG applications with high efficiency and low harmonic distortion. In future studies, the designed converter is planned to be used for energy management in MG applications.

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