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New Full-Wave Rectifiers Based on the Plus-Type Second-Generation Current Conveyors

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ABSTRACT

Two new full-wave rectifiers (FWRs) based on two plus-type second-generation current conveyors are proposed in this paper. Also, the proposed FWR structures comprise two diodes and two grounded resistors without matching conditions. They are not affected from any bias voltage(s) and/or current(s); thus, they eliminate the need for extra circuitry. One of the proposed FWRs provides positive rectification, while the other offers negative rectification. Both proposed FWRs have high input impedance and gain. Simulation results are obtained through the SPICE program, and experimental results are provided.

1 | Introduction

Full-wave rectifiers (FWRs) are essential analog circuits widely utilized in many areas, for example, control, instrumentation, measurement, and so forth, as declared in [1–27]. Also, second-generation current conveyors (CCIIs) previously introduced in [28] have been found wide application realms [29–35]. CCIIs as current-mode active devices possess some superiorities, for instance, wide bandwidth, good linearity, big dynamic range, and so forth [36–40] when compared to voltage-mode (VM) ones such as operational amplifiers (OAs).

The FWR circuits, made by using only diodes, have limitations for low-level signals because of the threshold voltages of the diodes. Therefore, some FWR circuits in the literature have been proposed for rectification within the threshold voltage levels of the diodes [1–27]. These FWRs with active elements employ resistors, diodes, BJTs, and MOS transistors.

The drawbacks of the VM FWRs in [1–27] are the following: (i) Several FWRs in [1, 3–8, 11] do not have gain. (ii) The circuits in [5–13] do not have high input impedances. (iii) The configurations in [9, 10, 20] consist of more than two active devices. (iv) The FWRs in [6, 9–11, 16–19] employ different types of active devices. (v) Resistors of some FWRs in [1, 7–12, 15] require matching conditions. (vi) Floating resistors are used in [7–15]. (vii) Bias current(s)/voltage(s) are required in [2–6, 16, 19, 20, 23–27]. (viii) The circuits of [9–11] employ OAs; therefore, they suffer from slew-rate limitations. (ix) The circuit of [14] requires floating input voltage; thus, extra circuitry is needed. (x) The FWRs in [1–3, 6, 9, 10, 12, 16–22] can be constructed with more than two commercially active devices. (xi) The FWRs in [9–12, 15] use more than two resistors. (xii) The circuits of [22, 26] include more than two diodes. The features of the FWRs of [1–27] in the literature and the proposed plus-type CCII (CCII+)-based ones are given in Table 1. Also, other properties, such as linearity range, power dissipation, frequency range, and so forth, of the FWRs and the proposed ones are shown in Table 2.

In this paper, two FWRs are proposed. These FWRs are based on two CCII+s. One of the proposed FWRs provides positive rectification, while the other offers negative rectification. Both proposed FWR topologies use two resistors without resistor

TABLE 1 | A comparison table for the full-wave rectifiers.

References	# of active devices	# of resistors/# of diodes	Floating resistor(s) /floating input	Matching	High input impedances	Gain	Need bias voltages or currents	The use of OA	Technology	Power supply voltages (V)
Figure 2 in [1]	2 DVCC+	2/2	No/no	Yes	Yes	No	No	No	0.25 μm	±1.25
Figure 1 in [2]	1 DXCCII[b]	0/0	No/no	No	Yes	Yes	Yes	No	0.25 μm	±1.25
Figure 3 in [3]	2 DDCC	0/0	No/no	No	Yes	No	Yes	No	0.5 μm	±2.5
Figure 3 in [4]	2 CFOA[b]	0/0	No/no	No	Yes	No	Yes	No	0.25 μm	±1.25
Figure 1 in [5]	2 CCII+[b]	0/0	No/no	No	No	No	Yes	No	0.25 μm	±1.25
Figure 2 in [6]	1 CCII+, 1 CCII−[b]	0/0	No/no	No	No	No	Yes	No	0.35 μm	±1.5
Figure 2 in [7]	1 CCII−	2/2	Yes/no	Yes	No	No	No	No	0.35 μm	±1.65
Figure 2b in [8]	1 VCII	2/2	Yes/no	Yes	No	No	No	No	0.35 μm	±1.65
Figure 5 in [9]	1 CCII+, 2 OA	3/2	Yes/no	Yes	No	Yes	No	Yes	AD844, LM741	—
Figure 1b in [10]	3 AD633, 2 AD817, 1 AD711	10/0	Yes/no	Yes	No	Yes	No	Yes	AD817, AD633, AD711	±15
Figure 2b in [11]	1 CCII+, 1 OA	3/2	Yes/no	Yes	No	No	No	Yes	AD844, LM741	—
Figure 7 in [12]	1 CDTA[b]	3/0	Yes/no	Yes	No	Yes	No	No	0.18 μm	±1.5
Figure 5 in [13]	2 VC+	2/2	Yes/no	No	No	Yes	No	No	0.35 μm	±1.65
Figure 3 in [14]	2 CCII+[a]	2/0	Yes/yes	No	Yes	Yes	No	No	AD844, 2N2222	±12
Figure 3 in [15]	2 CCII+	3/2	Yes/no	Yes	Yes	Yes	Yes	No	AD844	±12
Figure 4a in [16]	1 MO-CCII, 1 DO-CCII	3/2	No/no	No	Yes	Yes	Yes	No	AD8656	—
Figure 2b in [17]	1 CCII+, 1 UVC	2/2	No/no	No	Yes	Yes	No	No	AD825	—
Figure 2a in [18]	1 CCII+, 1 DXCCII	2/2	No/no	No	Yes	Yes	No	No	0.35 μm	±2.5
Figure 1 in [19]	1 DO-CCCII, 1 ZCD	1/0	No/no	No	Yes	Yes	Yes	No	PR200N, NP200N	±1.2
Figure 4 in [20]	5 OTA	2/0	No/no	No	Yes	Yes	Yes	No	LM13600	±15
Figure 1 in [21]	1 CCCII[b]	1/0	No/no	No	Yes	Yes	No	No	0.35 μm	±1.5
Figure 2 in [22][c]	1 DO-CCII	2/4	No/no	No	Yes	Yes	No	No	0.18 μm	±1.25
Figure 2 in [22][d]	1 DO-CCII	2/4	No/no	No	Yes	Yes	No	No	0.18 μm	±1.25
Figure 3 in [23]	1 CCII+[a]	2/0	No/no	No	Yes	Yes	Yes	No	AD844, 2N3904, 2N3906	±10

(Continues)

TABLE 1 | (Continued)

References	# of active devices	# of resistors/# of diodes	Floating resistor(s) /floating input	Matching	High input impedances	Gain	Need bias voltages or currents	The use of OA	Technology	Power supply voltages (V)
Figure 3 in [24]	1 CCII+[a]	2/0	No/no	No	Yes	Yes	Yes	No	AD844, 2N3904, 2N3906	±10
Figure 6 in [25]	1 CCII+[a]	2/0	No/no	No	Yes	Yes	Yes	No	TL082, 2N3904, 2N3906	±10
Figure 3 in [26]	1 FDIO-OTA	0/4	No/no	No	Yes	Yes	Yes	No	0.5 μm	±5
Figure 1a in [27]	1 MVDTA[b]	1/0	No/no	No	Yes	Yes	Yes	No	0.18 μm	±0.9
This work	2 CCII+	2/2	No/no	No	Yes	Yes	No	No	0.18 μm	±1.65

Note: —: not given.
[a]Extra BJTs are utilized.
[b]Additional MOS transistors are used.
[c]For positive FWR.
[d]For negative FWR.

matching conditions and two diodes. Also, the proposed FWRs have high input impedances. The gains of the proposed circuits are adjusted with the grounded resistors; therefore, the proposed circuit does not need extra amplifiers. The MMBD101LT1G diodes produced by ON semiconductor are utilized in both proposed FWRs [41]. Numerous simulations are made by using the SPICE program. AD844s [42] are used in the experiments for the proposed FWRs.

The rest of this manuscript is organized as follows: After the proposed FWRs are treated in Section 2, parasitic and non-ideal gain effects are searched in Section 3. Numerous simulations and several experiments are given in Sections 4 and 5, respectively. This paper is concluded in Section 6.

2 | Proposed Circuits

The voltage–current relationships of the terminals of the CCII+ presented in Figure 1 are

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \end{bmatrix} \tag{1}$$

Considering the proposed FWR circuits in Figures 2 and 3, if $V_{in} > 0$, D_2 diode is turned on, and D_1 is cut-off. If $V_{in} < 0$, D_1 diode is turned on, and D_2 is cut-off. Output voltages for the FWRs in Figures 2 and 3 are, respectively, obtained by

$$V_{out} = \frac{R_2}{R_1}|V_{in}| \tag{2a}$$

$$V_{out} = -\frac{R_2}{R_1}|V_{in}| \tag{2b}$$

3 | Parasitic and Non-Ideal Gain Effects

As an example, the parasitic impedance and non-ideal gain effects are investigated for only positive FWR. In other words, parasitic impedance analyses are examined to see their impacts on the performance of the CCII+ based positive FWR. The CCII+ with parasitics and the proposed positive FWR with parasitics are shown in Figures 4 and 5, respectively. The CCII+ with parasitic elements and non-ideal gains are expressed as

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} sC_Y & 0 & 0 \\ \beta & R_X & 0 \\ 0 & \alpha & sC_Z + 1/R_Z \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{3}$$

where the values of R_X, C_Y, and C_Z are ideally zero, while R_Z is ideally infinity. In addition, β and α are ideally equal to unity, which are non-ideal voltage and current gains, respectively.

TABLE 2 | A comparison table for some other features of the full-wave rectifiers.

References	# of active device	Reported DC linearity range	Power dissipation	Reported frequency range
Figure 2 in [1]	2 DVCC+	−0.17 to 0.17 V	0.93 mW	Up to 1 MHz
Figure 1 in [2]	1 DXCCII[b]	−0.15 to 0.15 V	3.33 mW	Up to 1 MHz
Figure 3 in [3]	2 DDCC	−1 to 1 V	—	Up to 1 MHz
Figure 3 in [4]	2 CFOA[b]	−0.35 to 0.35 V	1.33 mW	Up to 1 MHz
Figure 1 in [5]	2 CCII+[b]	−0.05 to 0.05 V	—	Up to 0.25 MHz
Figure 2 in [6]	1 CCII+, 1 CCII−[b]	−0.3 to 0.3 V	—	Up to 1 MHz
Figure 2 in [7]	1 CCII−	−0.37 to 0.37 V	—	Up to 40 kHz
Figure 2b in [8]	1 VCII	−0.6 to 0.6 V	0.24 mW	Up to 1 MHz
Figure 5 in [9]	1 CCII+, 2 OA	−0.5 to 0.5 V	—	Up to 0.1 MHz
Figure 1b in [10]	3 AD633, 2 AD817, 1 AD711	−5 to 5 V	—	Up to 1 MHz
Figure 2b in [11]	1 CCII+, 1 OA	—	—	Up to 0.5 MHz
Figure 7 in [12]	1 CDTA[b]	—	1.12 mW	Up to 100 MHz
Figure 5 in [13]	2 VC+	−20 to 20 μA	1.38 mW	Up to 1 MHz
Figure 3 in [14]	2 CCII+[a]	−0.1 to 0.1 V	—	Up to 100 Hz
Figure 3 in [15]	2 CCII+	−1 to 1 V	—	Up to 1 MHz
Figure 4a in [16]	1 MO-CCII, 1 DO-CCII	−0.4 to 0.4 V	—	Up to 1 MHz
Figure 2b in [17]	1 CCII+, 1 UVC	−0.25 to 0.25 V	—	Up to 0.5 MHz
Figure 2a in [18]	1 CCII+, 1 DXCCII	−0.35 to 0.35 V	—	Up to 1 MHz
Figure 1 in [19]	1 DO-CCCII, 1 ZCD	−0.1 to 0.1 V	2.83 mW	Up to 10 MHz
Figure 4 in [20]	5 OTA	−5 to 5 V	—	Up to 50 kHz
Figure 1 in [21]	1 CCCII[b]	−0.5 to 0.5 V	1.18 mW	Up to 30 MHz
Figure 2 in [22][c]	1 DO-CCII	−0.3 to 0.3 V	1.49 mW	Up to 1 MHz
Figure 2 in [22][d]	1 DO-CCII	−0.3 to 0.3 V	1.49 mW	Up to 1 MHz
Figure 3 in [23]	1 CCII+[a]	−0.1 to 0.1 V	—	Up to 0.1 MHz
Figure 3 in [24]	1 CCII+[a]	−0.05 to 0.05 V	—	Up to 1 MHz
Figure 6 in [25]	1 CCII+[a]	−5 to 5 mV	—	Up to 0.1 MHz
Figure 3 in [26]	1 FDIO-OTA	−0.4 to 0.4 V	—	Up to 1 MHz
Figure 1a in [27]	1 MVDTA[b]	−0.35 to 0.35 V	0.84 mW	Up to 50 MHz
This work	2 CCII+	−0.4 to 0.4 V	6.38 mW	Up to 1 MHz

Note: —: not given.
[a]Extra BJTs are utilized.
[b]Additional MOS transistors are used.
[c]For positive FWR.
[d]For negative FWR.

If parasitics and non-ideal DC gains of the CCII+s are considered, both diodes are assumed to be ideal. For $V_{in}>0$, D_2 diode is turned on, and D_1 is cut-off. As a result, $V_{X1}=\beta_1\cdot V_{in}$, $I_{X1}=-V_{X1}/(R_1+R_{X1})$, $I_{Z1}=\alpha_1\cdot I_{X1}$, $I_{X2}=I_{Z2}=0$, and $V_{out}=-I_{Z1}\cdot(R_2//R_{Z1}//R_{Z2}//(1/sC_{Z1})//(1/sC_{Z2}))$. Similarly, if parasitics and non-ideal DC gains of the CCII+s are considered, both diodes are assumed to be ideal. For $V_{in}<0$, D_1 diode is turned on, and D_2 is cut-off. Thus, $V_{X1}=\beta_1\cdot V_{in}$, $I_{X1}=-V_{X1}/(R_1+R_{X1})$, $I_{Z1}=\alpha_1\cdot I_{X1}$, $I_{Z1}=I_a-I_{X2}$, $-V_{Z1}=I_a\cdot(R_{Z1}//(1/sC_{Z1}))$, $V_{X2}=V_{Y2}=0$, $V_{Z1}=I_{X2}\cdot R_{X2}$, $I_{Z2}=\alpha_2\cdot I_{X2}$, $V_{out}=-I_{Z2}\cdot(R_2//R_{Z2}//(1/sC_{Z2}))$. Therefore, the output voltages of the proposed positive FWR for $V_{in}>0$ and $V_{in}<0$ are, respectively, obtained as

$$V_{out}=\frac{\alpha_1\beta_1\left(R_2\,\|\,R_{Z1}\,\|\,R_{Z2}\,\|\left(\frac{1}{s(C_{Z1}+C_{Z2})}\right)\right)}{(R_1+R_{X1})}V_{in} \quad (4a)$$

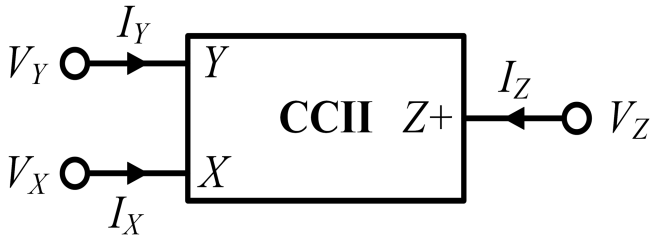

FIGURE 1 | Representation of the CCII+.

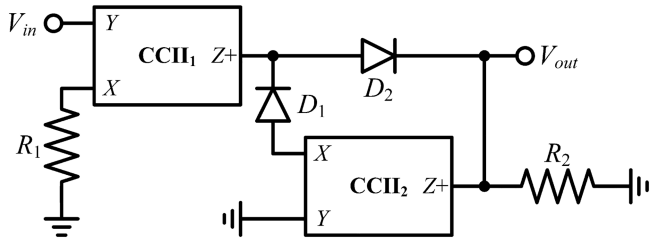

FIGURE 2 | The proposed positive FWR, based on the CCII+s.

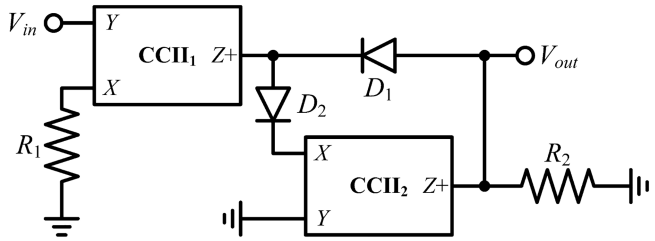

FIGURE 3 | The proposed negative FWR, based on the CCII+s.

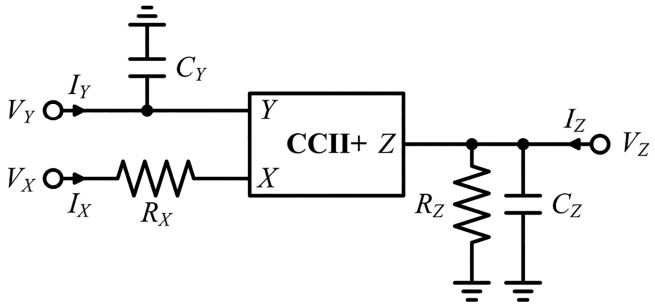

FIGURE 4 | The CCII+ with parasitics.

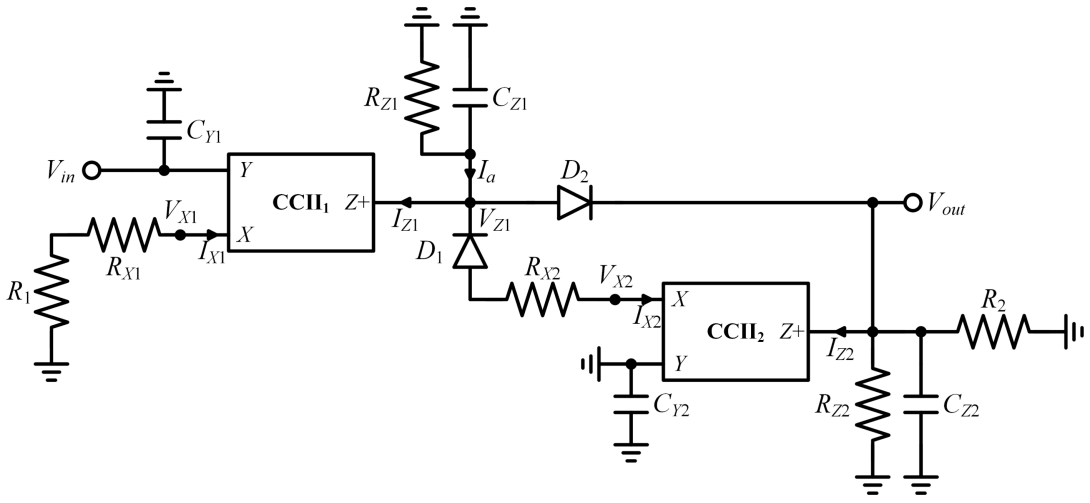

FIGURE 5 | The proposed positive FWR with parasitics.

$$V_{out} = -\frac{\alpha_1\alpha_2\beta_1\left(R_{Z1}\parallel\frac{1}{sC_{Z1}}\right)\left(R_2\parallel R_{Z2}\parallel\frac{1}{sC_{Z2}}\right)}{\left(R_1+R_{X1}\right)\left(\left(R_{Z1}\parallel\frac{1}{sC_{Z1}}\right)+R_{X2}\right)}V_{in} \tag{4b}$$

From (4a) and (4b), it can be observed that the effects of the parasitic impedances can be neglected if $R_1>>R_X$, $R_{Z1}\to\infty$, $R_{Z2}\to\infty$, $C_{Z1}\to 0$, and $C_{Z2}\to 0$. It is seen from (4a) and (4b) that the following constraints occur [43, 44]:

$$2\pi f\left(C_{Z1}+C_{Z2}\right) << \frac{1}{R_{Z1}\parallel R_{Z2}\parallel R_2} \tag{5a}$$

$$2\pi f C_{Z2} << \frac{1}{R_{Z2}\parallel R_2} \tag{5b}$$

$$2\pi f C_{Z1} << \frac{1}{R_{Z1}\parallel R_{X2}} \tag{5c}$$

From (5a), (5b), and (5c), the following frequency ranges are, respectively, obtained [45]:

$$f \le \frac{0.1}{2\pi}\frac{1}{\left(C_{Z1}+C_{Z2}\right)\left(R_{Z1}\parallel R_{Z2}\parallel R_2\right)} \tag{6a}$$

$$f \le \frac{0.1}{2\pi}\frac{1}{C_{Z2}\left(R_{Z2}\parallel R_2\right)} \tag{6b}$$

$$f \le \frac{0.1}{2\pi}\frac{1}{C_{Z1}\left(R_{Z1}\parallel R_{X2}\right)} \tag{6c}$$

Using a single pole model, frequency-dependent non-ideal gains of the CCII+ in the matrix (3) can be given below.

$$\alpha(\omega) = \frac{\alpha_o}{1+\frac{j\omega}{\omega_\alpha}} \tag{7a}$$

$$\beta(\omega) = \frac{\beta_o}{1 + \frac{j\omega}{\omega_\beta}} \tag{7b}$$

Here, β_o and α_o are non-ideal DC gains, while ω_β and ω_α are angular pole frequencies. If only these non-ideal gains are considered, the output voltage of the positive FWR in (4a) and (4b), respectively, becomes as

$$V_{out} = \frac{R_2}{R_1} \frac{\alpha_{o1}}{1 + \frac{j\omega}{\omega_{\alpha1}}} \frac{\beta_{o1}}{1 + \frac{j\omega}{\omega_{\beta1}}} V_{in} \tag{8a}$$

$$V_{out} = -\frac{R_2}{R_1} \frac{\alpha_{o1}}{1 + \frac{j\omega}{\omega_{\alpha1}}} \frac{\alpha_{o2}}{1 + \frac{j\omega}{\omega_{\alpha2}}} \frac{\beta_{o1}}{1 + \frac{j\omega}{\omega_{\beta1}}} V_{in} \tag{8b}$$

From (8), the resulting constraints are

$$\omega << \omega_{\alpha1} \tag{9a}$$

$$\omega << \omega_{\alpha2} \tag{9b}$$

$$\omega << \omega_{\beta1} \tag{9c}$$

The DC value transfer (p_{DC}) and RMS error (p_{RMS}), which are the important performance parameters of the FWRs, are utilized to show the accuracy of the FWRs. The value of the p_{DC} is ideally one, while the value of the p_{RMS} is zero. The equations of the p_{DC} and p_{RMS} are, respectively, given as [3].

$$p_{\mathrm{DC}} = \frac{\int_T V_{oa}(t)dt}{\int_T V_{oi}(t)dt} \tag{10a}$$

$$p_{\mathrm{RMS}} = \sqrt{\frac{\int_T \left[V_{oa}(t) - V_{oi}(t)\right]^2 dt}{\int_T V_{oi}^2(t)dt}} \tag{10b}$$

Here, $V_{oa}(t)$ and $V_{oi}(t)$ express the real and ideal output values of the FWR, respectively.

TABLE 3 | Aspect ratios of the CCII+ in Figure 6.

MOS transistors	W (μm)		L (μm)
PMOS	M_1–M_6, M_{11}, M_{12}	90	0.36
	M_7, M_8	6	
	M_{14}	40	
NMOS	M_{10}, M_{13}, M_{17}–M_{22}	45	
	M_{15}, M_{16}	2	
	M_9	30	

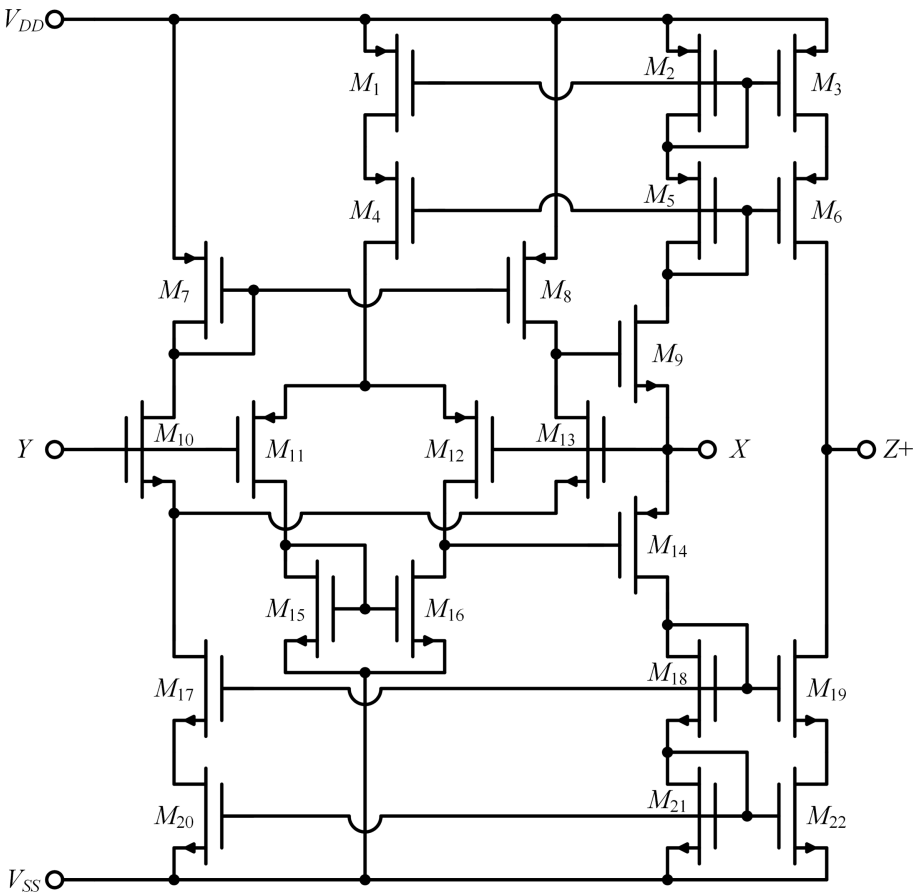

FIGURE 6 | The internal structure of the CCII+ derived from [46].

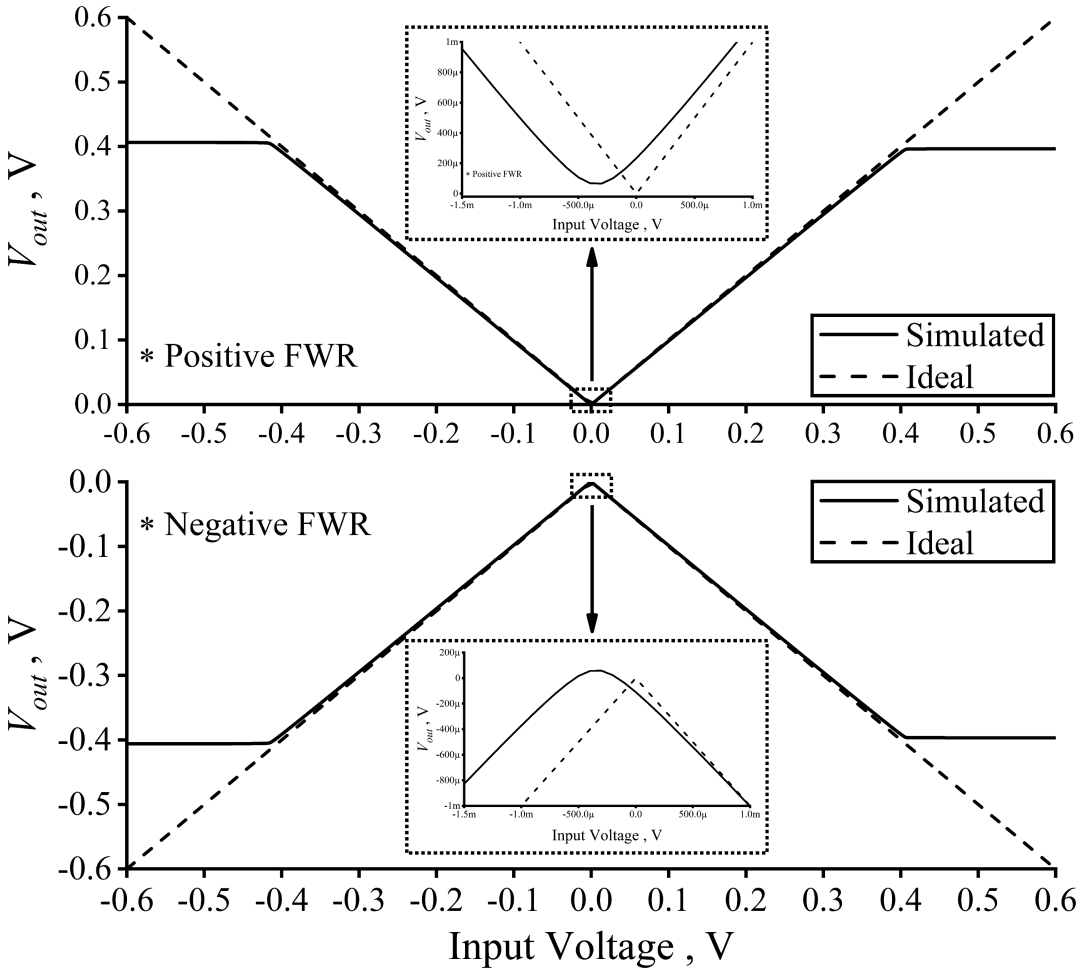

FIGURE 7 | DC analyses of the proposed FWRs based on the CCII+s.

TABLE 4 | Some performance parameters of the CCII+ in Figure 6.

Parasitic impedances of the CCII+	
$R_X \cong 4.16\,\Omega$	$R_{Z+} \cong 1.62\,\text{M}\Omega$
$C_Y \cong 98.54\,\text{fF}$	$C_{Z+} \cong 189.8\,\text{fF}$
Non-ideal gains of the CCII+	
$\beta_o = 0.9869$	$\alpha_o = 1.0003$
$f_\beta \cong 2.11\,\text{GHz}$	$f_\alpha \cong 297.4\,\text{MHz}$

4 | Simulations

The CCII+ used in the proposed FWRs of Figures 2 and 3 are shown in Figure 6, which is derived from [46]. The parasitic impedances of Figure 6, R_X and R_{Z+}, are calculated in Equation (11). This CCII+ has self-biasing property. Aspect ratios of all the MOS transistors of the CCII+ in Figure 6 are taken as in Table 3. In the proposed FWRs, 0.18 μm TSMC CMOS technology parameters [47] are utilized. The supply voltages V_{DD} and V_{SS} of the CCII+ are taken as ±1.65 V. The parasitics and non-ideal gains values of the CCII+ of Figure 6 are given in Table 4. All the simulation results are obtained through the OrCAD PSpice program.

$$R_X \cong \left(g_{m9}g_{m13}\left(r_{O8} \| r_{O13}\right)\right)^{-1} \| \left(g_{m12}g_{m14}\left(r_{O12} \| r_{O16}\right)\right)^{-1} \quad (11a)$$

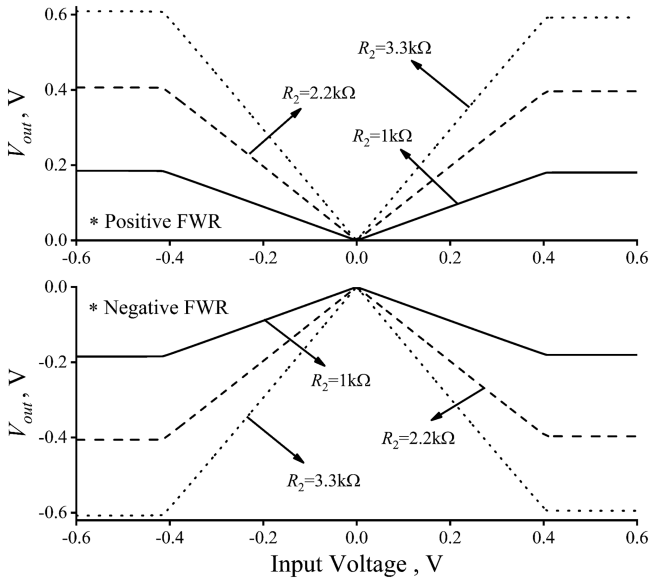

FIGURE 8 | DC analyses of the proposed FWRs based on the CCII+s for different gains.

$$R_{Z+} \cong \left(r_{O3}r_{O6}g_{m6}\right) \| \left(r_{O19}r_{O22}g_{m19}\right) \quad (11b)$$

In Figure 7, DC analyses are exhibited for the proposed FWRs in which the passive elements are taken as $R_1 = R_2 = 2.2\,\text{k}\Omega$. Thus, the

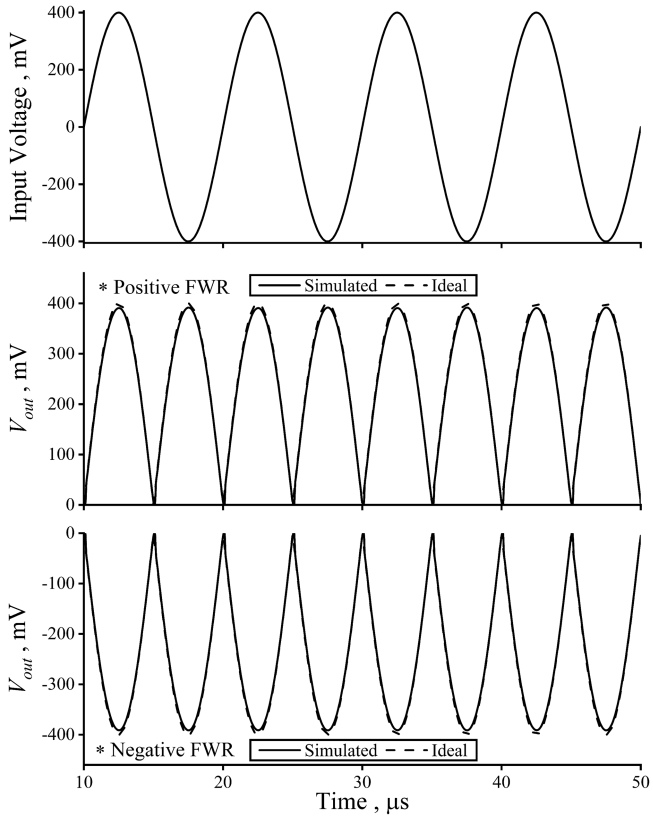

FIGURE 9 | Transient analyses of the FWRs based on the CCII+s at 100 kHz.

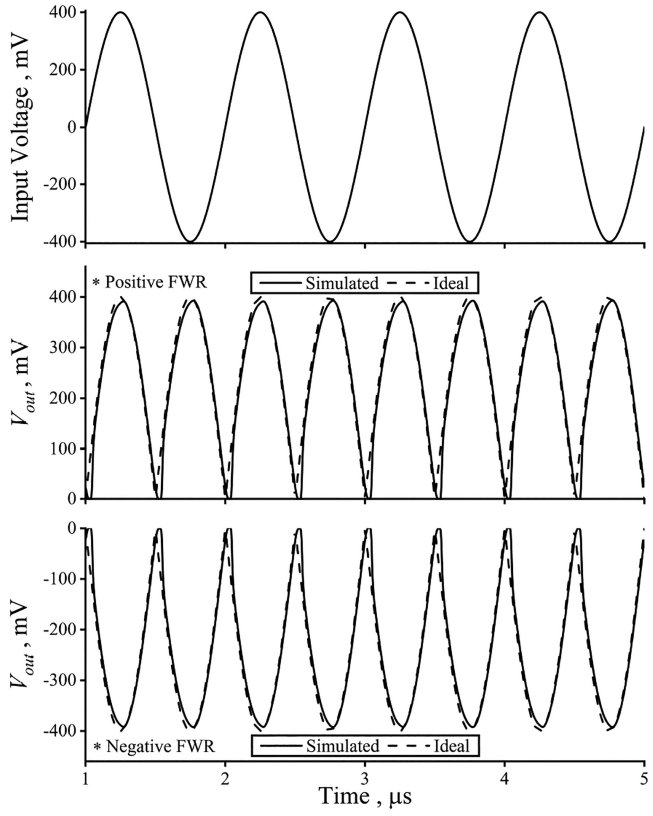

FIGURE 10 | Transient analyses of the FWRs based on the CCII+s at 1 MHz.

gain is computed as unity, as an example. The simulated and ideal outputs given in Figure 7 are obtained, where the input voltage values are varied from −0.6 to 0.6 V. Furthermore, zero crossing areas of the proposed FWRs can be seen in Figure 7, which shows the proposed FWRs can work with very small input voltages. If $R_1 = 2.2\,k\Omega$ and R_2 of the proposed FWRs in Figures 2 and 3 are, respectively, selected as 1 kΩ, 2.2 kΩ, and 3.3 kΩ, the outputs are obtained as seen in Figure 8. For both the proposed FWRs, transient analyses are respectively given in Figures 9 and 10, where a sinusoidal input voltage with 400-mV peak is applied, and $R_1 = R_2 = 2.2\,k\Omega$ is taken. In Figures 9 and 10, the selected frequencies are, respectively, 100 kHz and 1 MHz. The power consumption of each of the FWRs is computed as 6.38 mW.

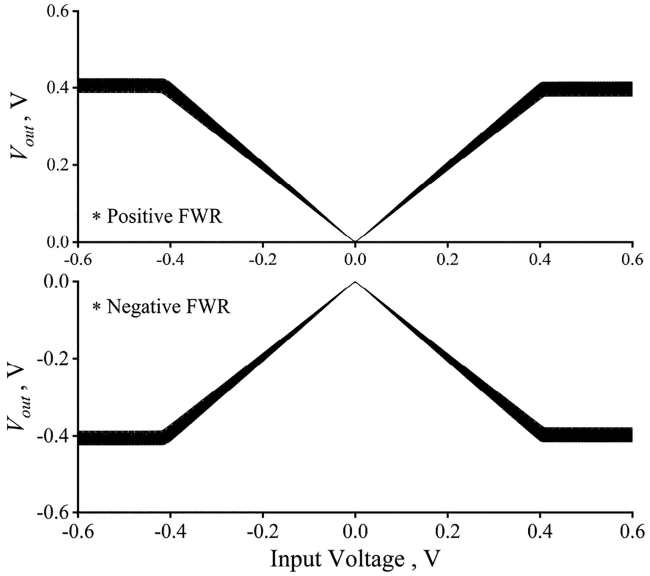

FIGURE 11 | MC analysis for the FWRs based on the CCII+s.

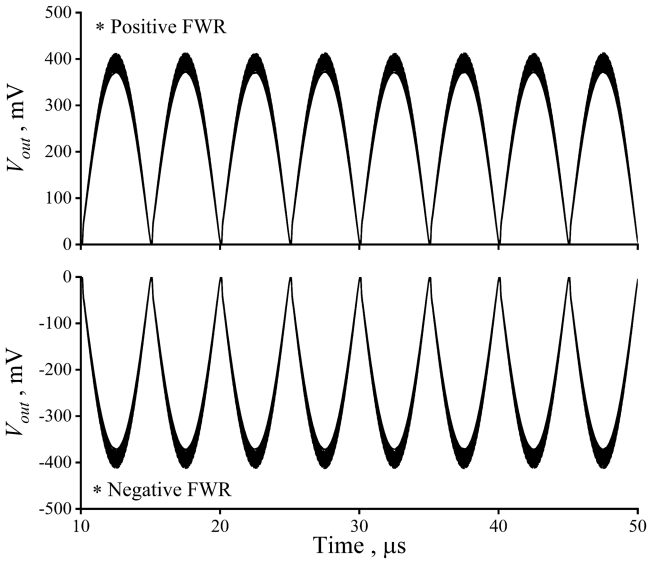

FIGURE 12 | MC analysis for the FWRs based on the CCII+s results in time domain.

As shown in Figures 9 and 10, if the gain is chosen as unity, the proposed FWRs appropriately operate up to about 400 mV. As demonstrated in Figure 9, the proposed FWR in Figure 2 deviates from the ideal response approximately 9.2 mV in the positive cycle and about 8.3 mV in the negative cycle, while the proposed FWR in Figure 3 deviates from the ideal response approximately 8.8 mV in the positive cycle and about 8.7 mV in the negative cycle. As demonstrated in Figure 10, the proposed FWR in Figure 2 deviates from the ideal response about 12.1 mV in the positive cycle and about 10.9 mV in the negative cycle, while

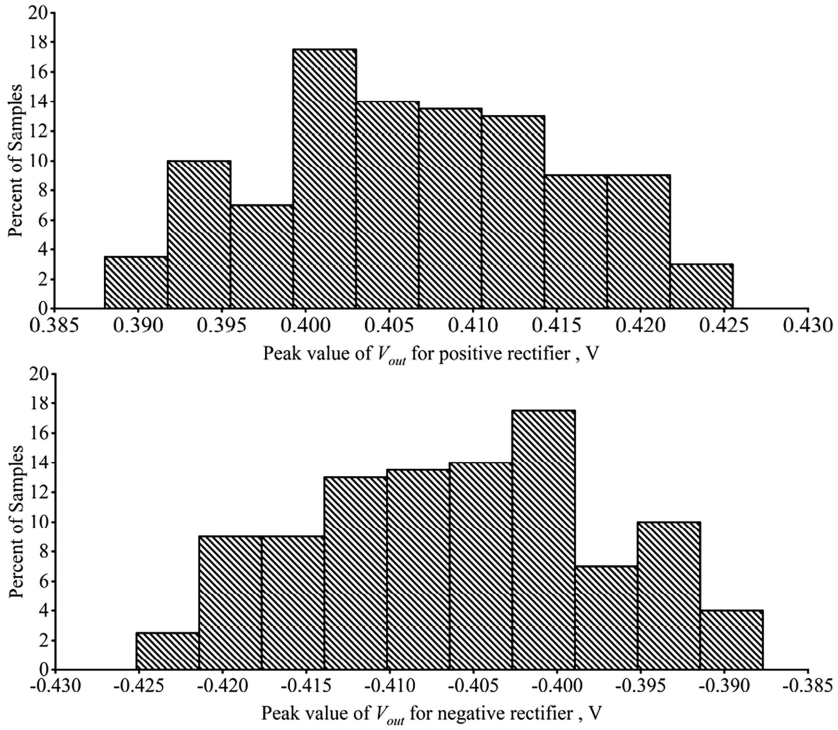

FIGURE 13 | MC analysis histogram results of the FWRs for peak value of the output voltages.

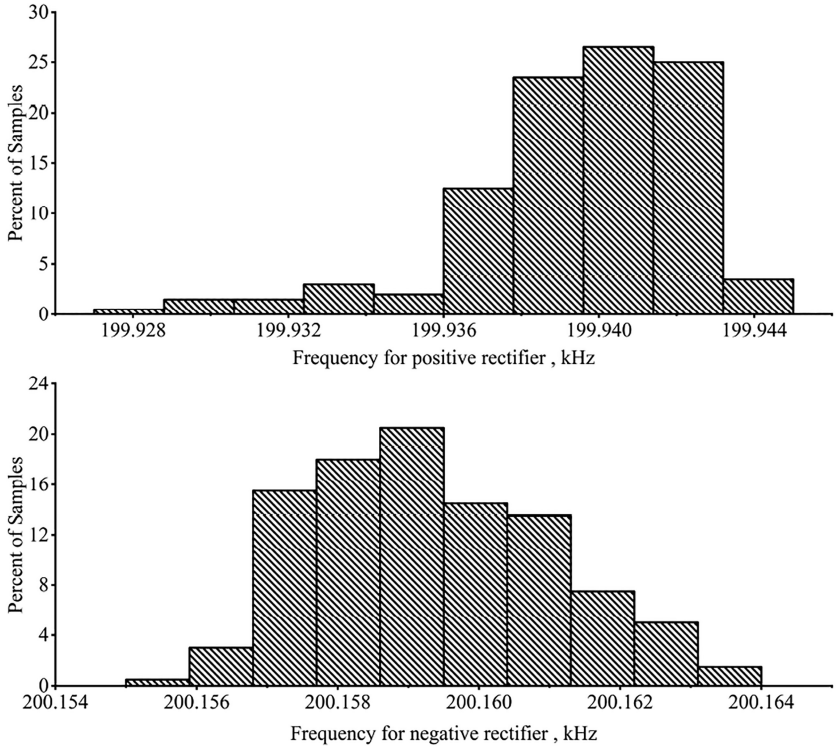

FIGURE 14 | MC analysis histogram results of the FWRs for the frequency of the output voltages.

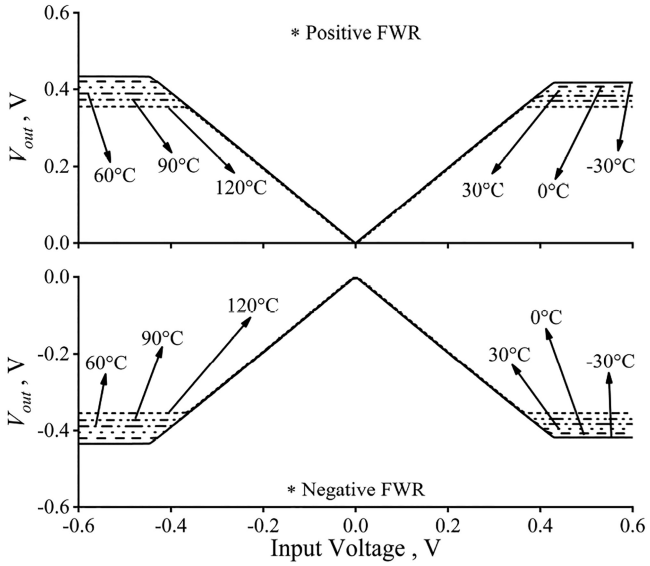

FIGURE 15 | DC temperature analysis results of the proposed FWRs based on the CCII+s.

the proposed FWR in Figure 3 deviates from the ideal response approximately 11.8 mV in the positive cycle and about 11.2 mV in the negative cycle. One observes from Figures 9 and 10 that the CCII+ based FWRs operate properly up to about 1 MHz. In Figure 11, DC Monte Carlo (MC) analyses are given for the proposed FWRs based on the CCII+s in which the resistors are taken as $R_1 = R_2 = 2.2\,k\Omega$, and the uniform deviations for all the resistors are selected as 3%. Further, MC analyses in the time domain are shown in Figure 12, where a sinusoidal input voltage with 400 mV peak is applied at 100 kHz. The histogram results for the peak value and the frequency of the output voltages of the FWRs are respectively demonstrated in Figures 13 and 14. The mean peak value of the positive FWR in Figure 14 is calculated as 0.40636 V via the PSpice program, while the mean peak value of the negative FWR is found to be −0.406029 V. The mean frequencies of the positive and negative FWRs in Figure 15 are obtained as 199.939 kHz and 200.159 kHz, respectively. The temperature analysis results are shown in Figure 15, in which the temperature is varied from –30°C to 120°C. Also, p_{DC} and p_{RMS} versus frequency are shown in Figure 16, where the input voltage is selected as 800 mV peak-to-peak for the CCII+ based

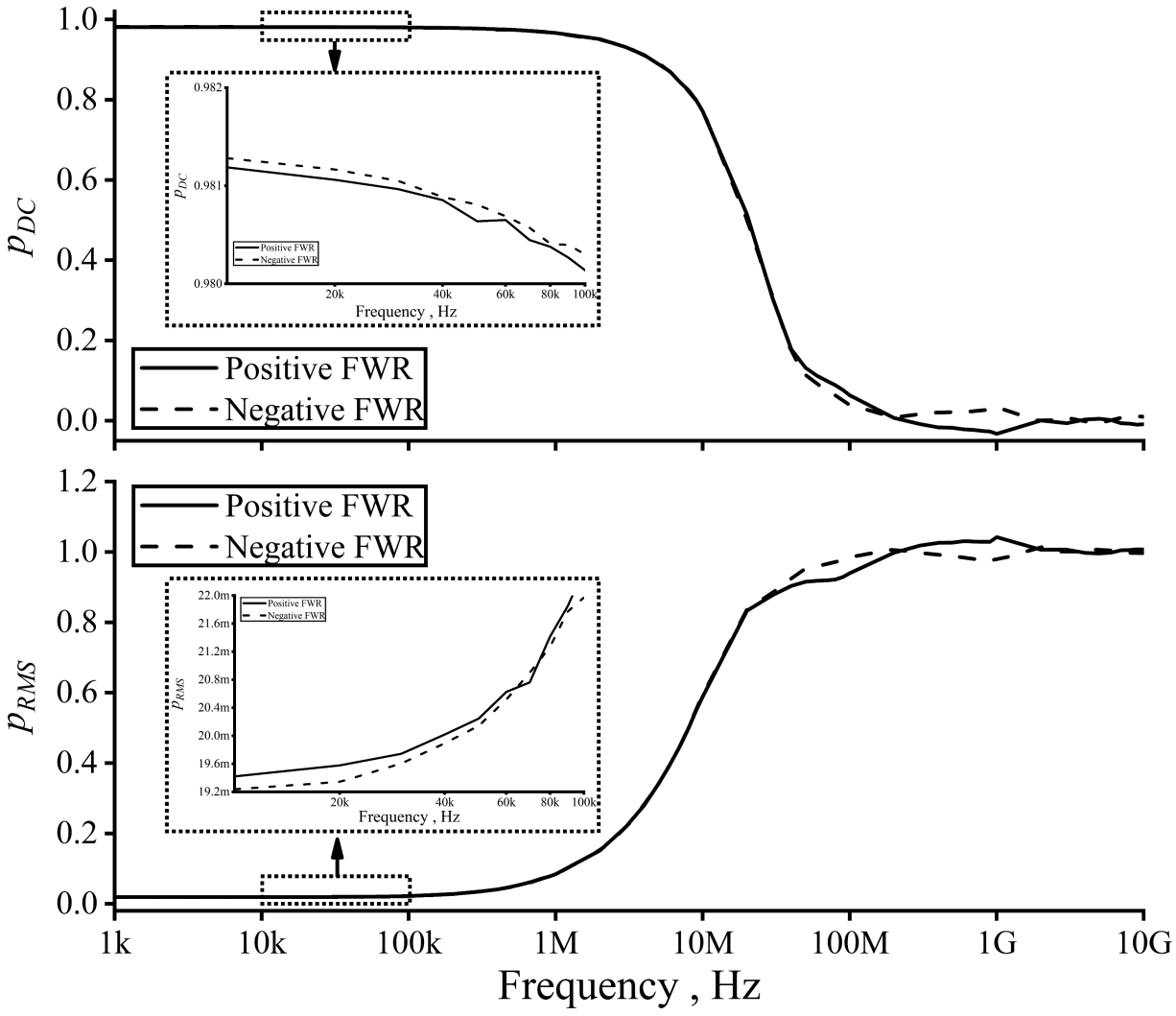

FIGURE 16 | p_{DC} and p_{RMS} against frequency.

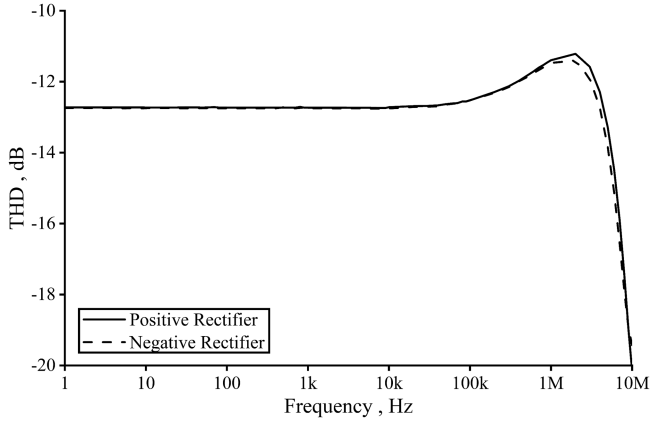

FIGURE 17 | THD results of the FWRs against frequency.

FWRs. According to [10, 18], the total harmonic distortion (THD) variations of the proposed FWRs are investigated. THD against the frequency results of the rectified voltages are indicated in Figure 17, in which the magnitude of the input voltage is selected as 0.4 V. The noise calculation of the CCII was given in [48] before. Also, the output noises of the rectifiers are shown in Figure 18.

5 | Experimental Results

The experimental tests for both proposed FWRs based on the CCII+s are performed by using two AD844s. In other words, the CCII+ can be obtained commercially by using one AD844. The experimental setup for the positive FWR is depicted in Figure 19.

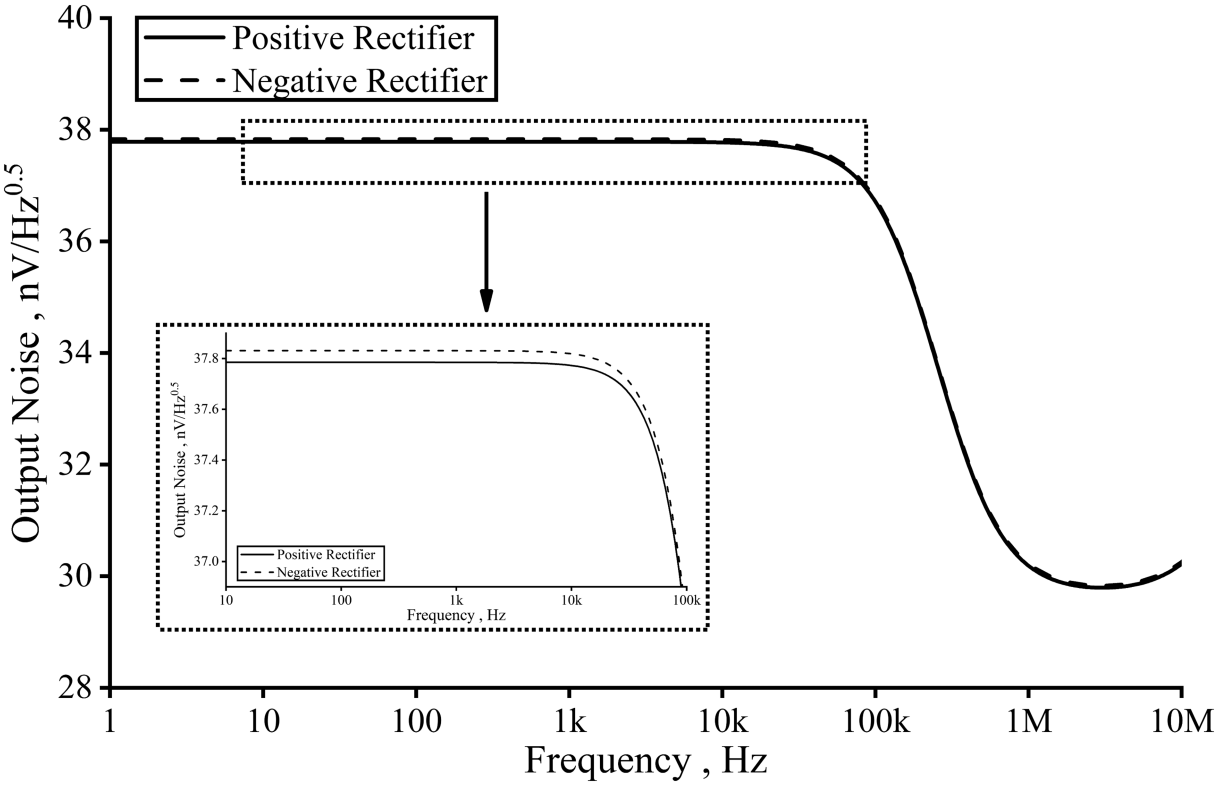

FIGURE 18 | Output noises of the FWRs against frequency.

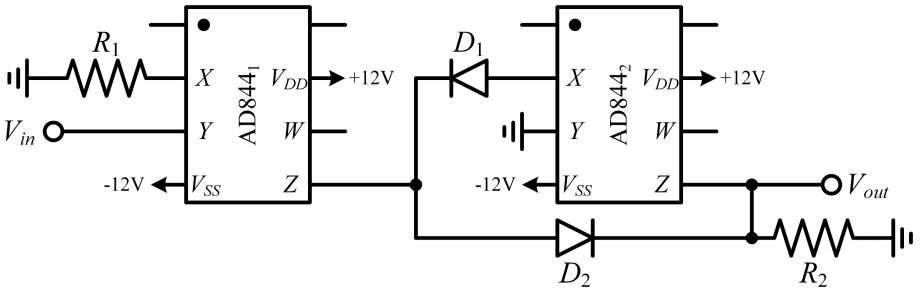

FIGURE 19 | Experimental setup for the proposed positive FWR.

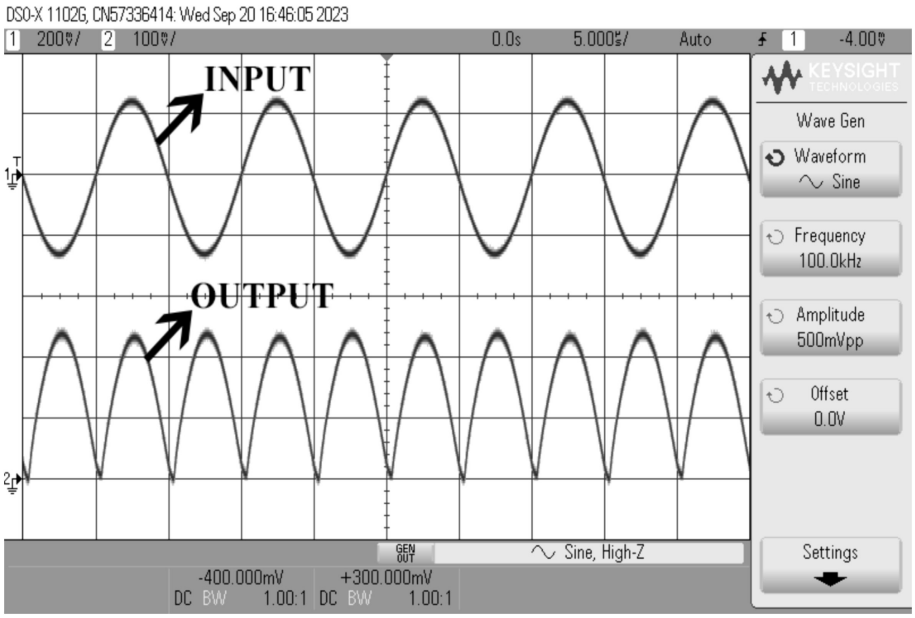

FIGURE 20 | Experimental result for the proposed positive FWR.

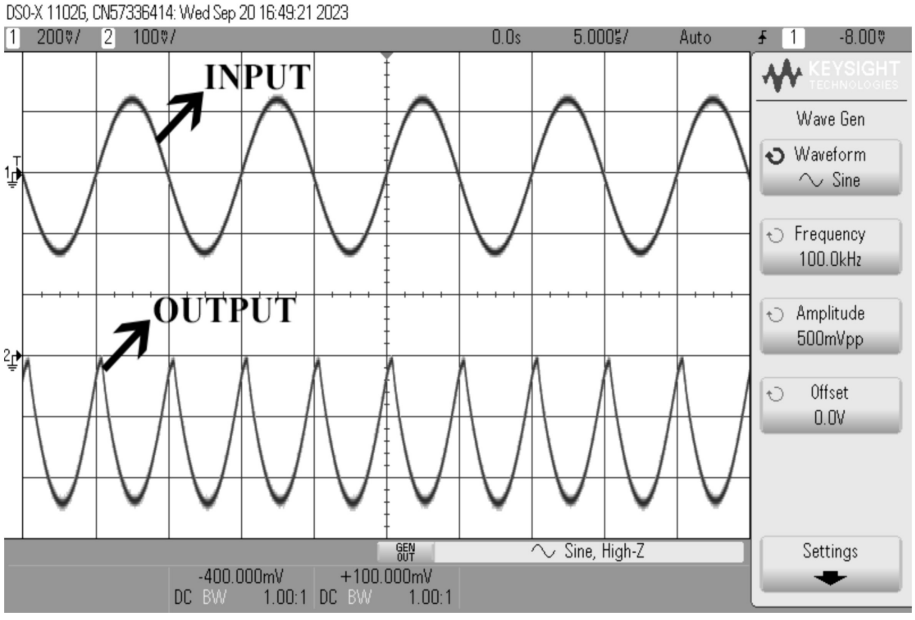

FIGURE 21 | Experimental result for the proposed negative FWR.

The supply voltages of the AD844s in the experiments are taken as ±12V. The applied sinusoidal input voltage signals for both FWRs in Figures 2 and 3 are selected as 500 mV peak-to-peak at 100 kHz. The passive elements for both FWRs of Figures 2 and 3 are taken as 2.2 kΩ; thus, the gain is obtained as unity. The results for both FWRs of Figures 2 and 3 are respectively shown in Figures 20 and 21. Also, experiments of the DC analyses of the proposed FWRs are achieved, where DC input voltages from −10 to 10 V are applied. The results of DC analyses are shown in Figure 22. In addition, phase and gain errors are investigated in the experiment tests, where the amplitude of the sinusoidal input voltage is selected as 250 mV, and the frequencies of the input voltage are chosen from 1 kHz to 1 MHz. In Figure 23, the phase and gain error results are shown.

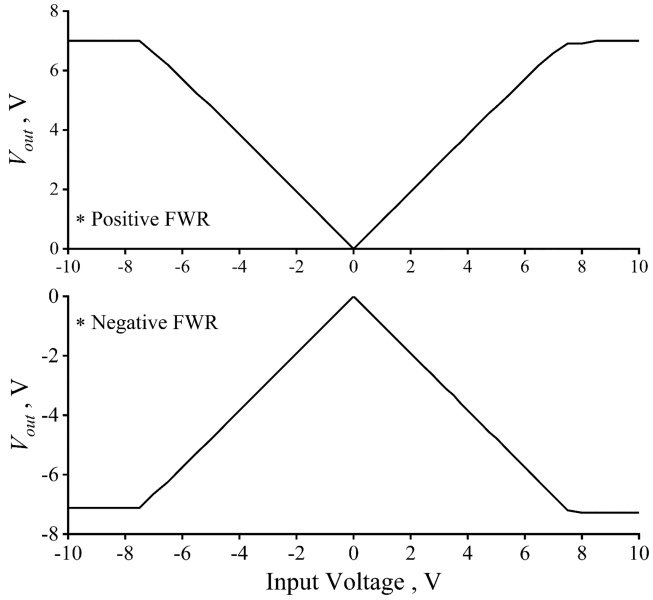

FIGURE 22 | Experimental results of the DC analyses for the proposed FWRs.

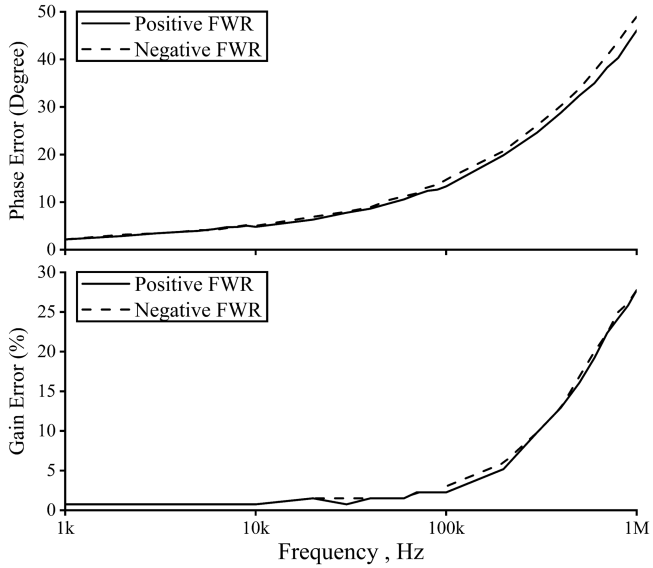

FIGURE 23 | Phase and gain error results of the proposed FWRs.

6 | Conclusion

The proposed FWRs based on the CCII+s have all the 10 features below. High input impedance, usage of two active elements, construction with two AD844s, no passive element matching condition, no use of floating passive elements, having gains, no need of any bias current(s)/voltage(s), not having different types of active devices, no need to use floating input voltage, no use OA. However, they need voltage followers for low output impedances. Additionally, they cannot provide positive and negative rectifications simultaneously. Several simulations using the SPICE program and some experiments prove the theory well. Nonetheless, the difference can be attributed to the non-idealities of the CCII+s, diodes, and AD844s.

Acknowledgments

The circuits of this manuscript were previously published in [49] as the PhD thesis.

Data Availability Statement

Data sharing is not applicable to this article as no datasets were generated or analyzed during the current study.

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