International Journal of Circuit Theory and Applications

WILEY

BRIEF REPORT OPEN ACCESS

Current-Mirror Based Filters With Reduced Circuit Complexity

Julia Nako[1] | Costas Psychalinos[1] | Shahram Minaei[2] | Erkan Yuce[3]

[1]Physics Department, Electronics Laboratory, University of Patras, Rio Patras, Greece | [2]Department of Electrical and Electronics Engineering, Dogus University, Istanbul, Türkiye | [3]Electrical and Electronics Engineering Department, Pamukkale University, Denizli, Türkiye

Correspondence: Costas Psychalinos (cpsychal@upatras.gr)

Received: 8 November 2024 | **Revised:** 17 December 2024 | **Accepted:** 29 December 2024

Funding: The publication of the article in OA mode was financially supported by HEAL-Link.

Keywords: analog integrated circuits | analog filters | analog signal processing | current-mirrors | current-mode filters

ABSTRACT

In this Letter, we propose a novel current-mirror-based lossless integration stage. The proposed stage is derived from the lossy integration counterpart by simply incorporating an additional DC current source. The unique offered contribution is the reduction of the circuit complexity in the resulting current-mode systems, where the introduced integrator is utilized. This is verified through the performed comparison with the corresponding stage, which is already introduced in the literature. A multiple-output biquad filter is designed using the proposed lossless integrator, and its performance is evaluated through the utilization of the Cadence IC design suite.

1 | Introduction

Current-mirrors have relatively simple structures [1, 2], offering reduced chip area, DC power dissipation and capability of high frequency operation, due to the absence of the compensation requirement [3–18]. The aforementioned benefits make them suitable candidates for implementing current-mode signal processing systems [19–27].

Although the implementation of a current-mirror-based lossy integrator is easy, performed just by adding an external capacitor at the common-gate connection of the employed MOS transistors, as it is shown in Figure 1a, this is not the case for implementing a lossless integrator. More specifically, in addition to the external capacitor, extra branches must be added; one of them realizes the output current copying, while the other two construct an extra current-mirror stage required for inverting the copied output current and fed it back to the input terminal. The resulting circuitry is depicted in Figure 1b. This solution suffers from the following drawbacks: (a) increased circuit complexity, (b) increased number of transistors that must be matched, and (c) reduced maximum frequency of operation, caused by the cascade connection of the extra current-mirror at the output of the lossy integrator.

The aforementioned obstacles are overcome by the topology introduced in this Letter. This is achieved by adding only one DC current source in the core of the lossy integration stage, which actually neutralizes the input resistance of the integrator, making the stages to behave as a pure lossless integrator.

The Letter is organized as follows: the proposed topology is presented in Section 2, where its performance is evaluated by performing a study of the effect of nonidealities, and by post-layout simulation results. A filter design example is presented in Section 3, and the performance of the resulting structure is evaluated in both frequency-domain and time-domain. Section 4 concludes the main derivations of this work.

2 | Proposed Lossless Integrator Realization

2.1 | Proposed Topology

Starting from the conventional implementation of a current-mirror based lossy integrator which is depicted in Figure 1a, the corresponding lossless integrator topology is demonstrated in Figure 1b, where an extra current-mirror is utilized towards this purpose [1, 2]. Assuming that the transistors M_{n1} and M_{n2} are matched (i.e., $g_{m,Mn1} = g_{m,Mn2} \equiv g_m$), the realized transfer functions are

$$H_1(s) = \frac{i_{out}}{i_{in}} = \frac{1}{\tau s + 1}, \tag{1a}$$

$$H_2(s) = \frac{i_{out}}{i_{in}} = \frac{1}{\tau s}, \tag{1b}$$

respectively. The time constant in (1a)–(1b) is given by the formula: $\tau = C_1/g_m$.

The drawbacks of the topology in Figure 1b, mentioned in the previous Section, can be overcome by the proposed structure in Figure 2a, which is directly resulting from the lossy integrator circuitry just by adding an extra DC current source. In this way, the input current i_{in} feeds only the capacitor C_1 and is converted into a voltage $v_{in} = i_{in}/C_1 s$. The transistor M_{n2} performs the required voltage-to-current (V/I) conversion according to the formula $i_{out} = g_{m,Mn2} v_{in}$; consequently, the realized transfer function is that in (1b) with the realized time constant given by the formula: $\tau = C_1/g_{m,Mn2}$.

2.2 | Effect of the Nonidealities

In order to study the effect of the nonidealities in the behavior of the topology in Figure 2a, let us consider the small-signal equivalent circuit depicted in Figure 2b. The resistances $r_{ds,p}$, and $r_{ds,n}$ represent the output resistances of the MOS transistors which implement the required DC current sources of the input branch. Assuming for simplicity that the condition $g_m r_{ds} > > 1$ is valid, then the following general simplifications could be made: $(1/g_m)//r_{ds} \simeq 1/g_m$ and $1/g_m + r_{ds} \simeq r_{ds}$.

Therefore

$$v_{in} = i_{in} \frac{r_{ds,n}//r_{ds,p}}{(r_{ds,n}//r_{ds,p})C_1 s + 1}. \tag{2}$$

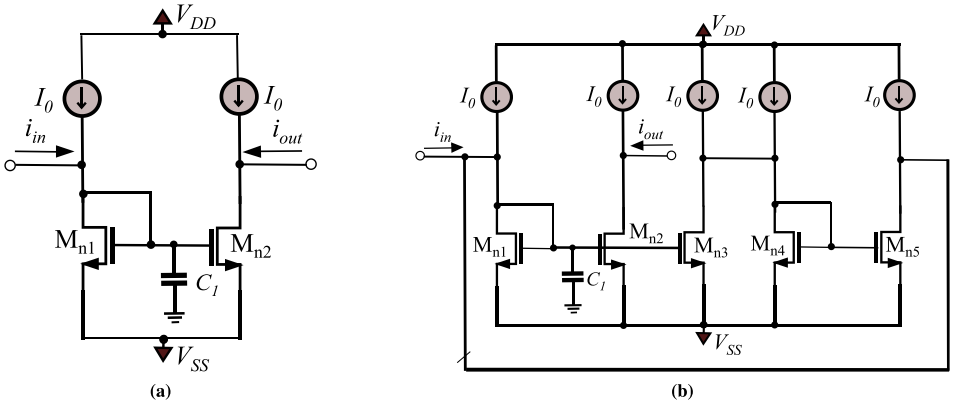


FIGURE 1 | Conventional implementation of current-mode (a) lossy integrator and (b) lossless integrator using current-mirrors.

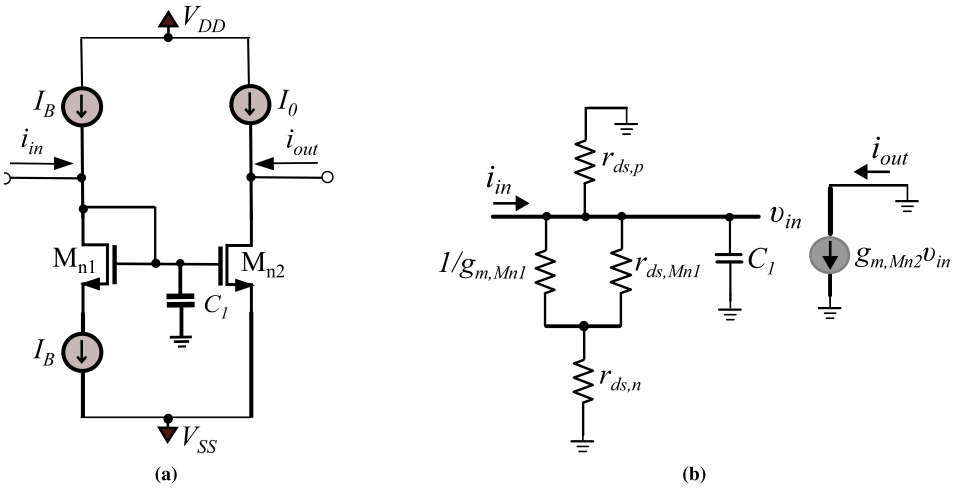


FIGURE 2 | (a) Proposed implementation of a current-mode lossless integrator and (b) its associated small-signal-model containing MOS transistors imperfections.

Using (2) and the formula $i_{out} = g_{m,Mn2}v_{in}$, the resulting transfer function becomes

$$H(s) = \frac{g_{m,Mn2}(r_{ds,n}//r_{ds,p})}{(r_{ds,n}//r_{ds,p})C_1 s + 1}. \quad (3)$$

According to (3), the topology behaves as a low-pass filter with maximum gain equal to $g_{m,Mn2}(r_{ds,n}//r_{ds,p})$ and an extremely low cut-off frequency given by the formula: $\omega_c = 1/(r_{ds,n}//r_{ds,p})C_1$.

TABLE 1 | Performance comparison results between the proposed topology and its conventional counterpart.

Performance factor	Conventional (Figure 1b)	Proposed (Figure2a)
Number of transistors	10	5
Power dissipation	$5(V_{DD} - V_{SS})I_0$	$(V_{DD} - V_{SS}) \cdot (I_0 + I_B)$
Minimum supply voltage	$V_{TH} + V_{DS,sat}$	$V_{TH} + 2V_{DS,sat}$
Minimum input voltage	V_{TH}	$V_{TH} + V_{DS,sat}$
Minimum output voltage	$V_{DS,sat}$	$V_{DS,sat}$
Matching requirement	YES	NO

V_{TH}: threshold voltage of MOS transistor
$V_{DS,sat}$: gate-overdrive voltage of MOS transistor

In addition, the unity gain frequency of the integrator will be given by

$$\omega_0 = \frac{g_{m,Mn2}}{C_1}\sqrt{1 - \left(\frac{1}{g_{m,Mn2}(r_{ds,n}//r_{ds,p})}\right)^2}. \quad (4)$$

According to (4), the unity gain frequency becomes lower than that which corresponds to the ideal case (i.e., $g_{m,Mn2}/C_1$), due to the presence of the output resistance of the current sources in the input branch.

With regards to the phase response, it becomes

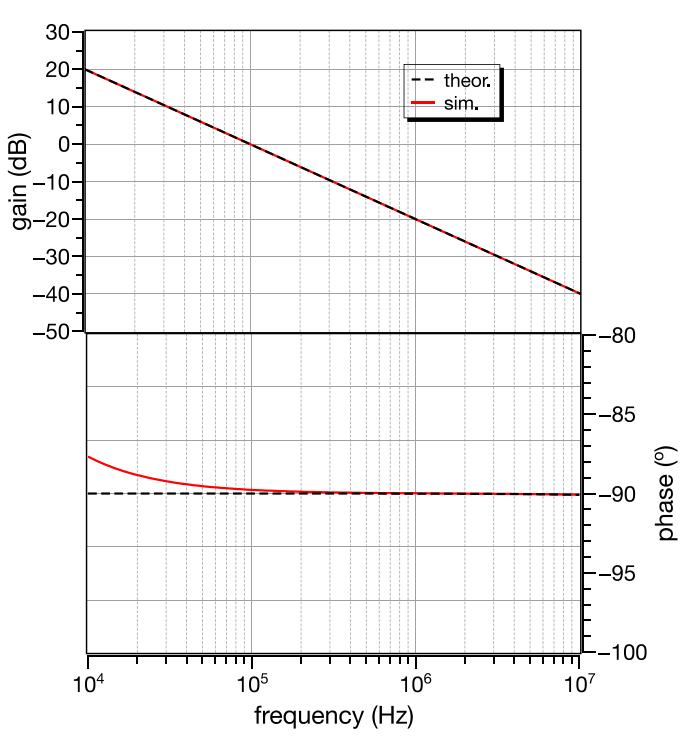
$$\arg H(\omega) = -\tan^{-1}\left[(r_{ds,n}//r_{ds,p})C_1\omega\right]. \quad (5)$$

Inspecting (4)–(5), it is readily obtained that in the case of ideal current sources (i.e., $r_{ds,n}//r_{ds,p} \to \infty$), the unity gain frequency becomes equal to $g_{m,Mn2}/C_1$, while the phase response is constant and equal to $-\pi/2$.

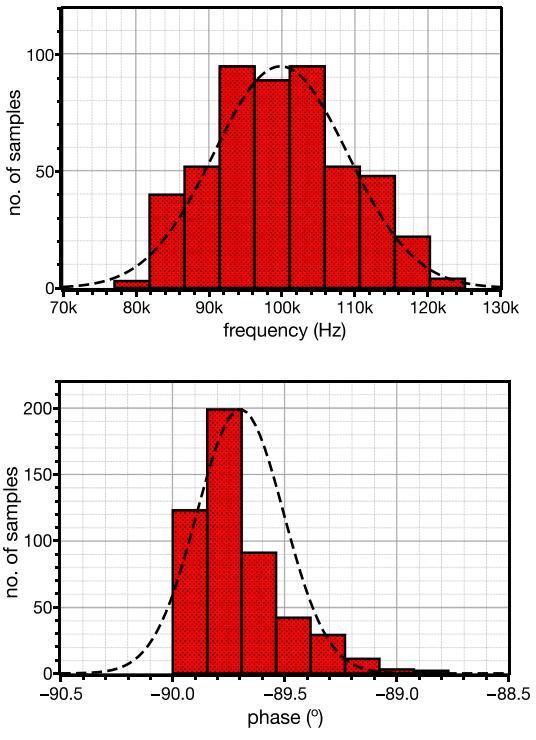
As the I_B current sources are implemented using PMOS and NMOS devices, which inherently have different mobilities, and are assumed to be matched, the impact of current mismatch on the performance of the proposed circuit will be that presence of an offset current proportional to the mismatch between these current sources.

2.3 | Performance comparison and evaluation

Assuming that each one of the DC current sources is implemented by a MOS transistor, the performance comparison results between



(a)



(b)

FIGURE 3 | Evaluation of the performance of the proposed lossless integrator at post-layout level. (a) Gain and phase responses and (b) Monte Carlo analysis histograms of the unity gain frequency (top) and the phase at this frequency (bottom).

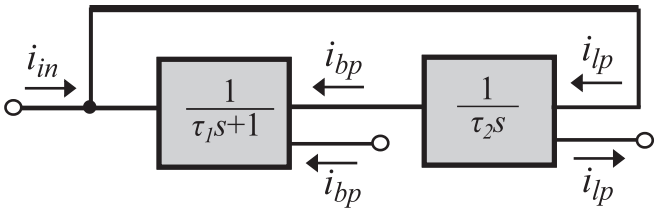


FIGURE 4 | Functional block diagram (FBD) of a current-mode two-integrator loop biquad filter.

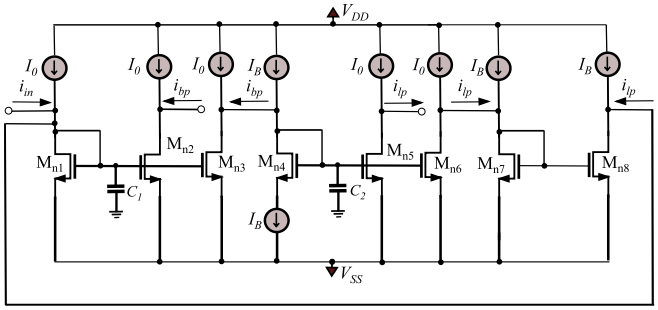


FIGURE 5 | Implementation of the FBD in Figure 4, using the proposed lossless integrator.

the proposed topology in Figure 2a and its conventional counterpart in Figure 1b are summarized in Table 1. From the provided results, it is readily obtained the achieved reduction of the circuit complexity and DC power dissipation. In addition, there is not any matching requirement between the transistors M_{n1} and M_{n2}, increasing the sensitivity performance of this topology. The fact that the topology in Figure 1a can be easily derived from that in Figure 2a, just by removing the lower DC current source, makes it versatile and could be considered as an easily re-configurable stage. The price paid for these achievements is the increased minimum supply voltage and input voltage requirements.

It must be mentioned at this point that the comparison is restricted between Figures 1b and 2a, because they have an original-improved relationship and, therefore, fair comparison results are derived. There are enhanced current-mirror topologies in the literature, where performance factors such as the input/output impedance have been improved, and the application of the presented concept in these topologies is included in our future research plans.

The behavior of the proposed lossless integrator is evaluated using the Cadence IC design suite and transistors models

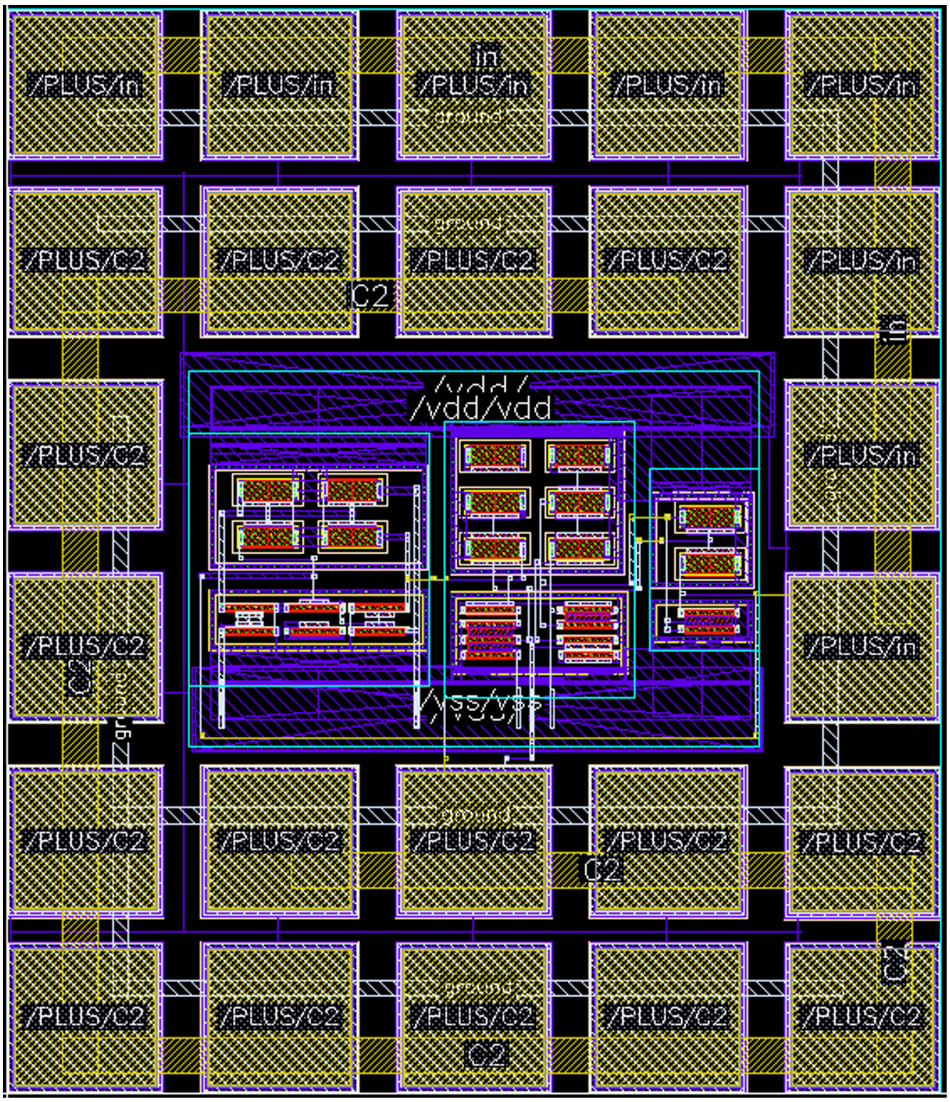


FIGURE 6 | Layout design of the biquad filter in Figure 5.

provided by the AMS 0.35μm CMOS process design kit. The utilized bias scheme is $V_{DD} = -V_{SS} = 1.5V$, while $I_B = 1$ μA and $I_0 = 5.44$ μA. The aspect ratio of the nMOS and pMOS transistors are 1 μm/10 μm and 4 μm/10 μm, including those which are employed for realizing the required DC current sources. The resulting value of the transconductance of M_{n2} is $g_{m,Mn2} = 10.35$ μS; therefore, $C_1 = 16.47$ pF for achieving a unity-gain frequency equal to 100 kHz.

The derived gain and phase responses of the integrator are depicted in Figure 3a with the corresponding theoretically predicted ones given by dashes. The simulated unity gain frequency is 99.7 kHz, while the associated phase at this frequency is −89.8°, close to the corresponding theoretical values. The sensitivity performance of the stage is evaluated using the Monte Carlo analysis tool, for $N = 500$ runs. The resulting statistical histograms about the unity gain frequency and the phase at this frequency, considering the effect of both the process parameters variation and MOS transistors parameters mismatching, are given in Figure 3b. The values of the standard deviation of the considered performance factors are 9.2 kHz, and 0.2°, respectively.

3 | Application Design Example

The proposed lossless integration stage could be utilized for implementing a two-integrator loop multiple output current-mode biquad, by employing the follow-the-leader-feedback (FLF) scheme depicted in Figure 4. The resulting topology is demonstrated in Figure 5, and the realized low-pass (LP) and band-pass (BP) filter functions are respectively found as

$$H_{lp}(s) = \frac{i_{lp}}{i_{in}} = \frac{\frac{1}{\tau_1\tau_2}}{s^2 + \frac{1}{\tau_1}s + \frac{1}{\tau_1\tau_2}}, \tag{6}$$

$$H_{bp}(s) = \frac{i_{bp}}{i_{in}} = \frac{\frac{1}{\tau_1}s}{s^2 + \frac{1}{\tau_1}s + \frac{1}{\tau_1\tau_2}}, \tag{7}$$

with $\tau_1 = C_1/g_{m,Mn2}$ and $\tau_2 = C_2/g_{m,Mn5}$ being the time constants realized by each one of the utilized integration stages.

The corresponding design equations are

$$\omega_0 = \frac{1}{\sqrt{\tau_1\tau_2}} \quad Q = \sqrt{\frac{\tau_1}{\tau_2}}, \tag{8}$$

with ω_0, Q being the frequency and the quality factor of the poles, respectively.

A Butterworth low-pass filter response is achieved for $Q = 1/\sqrt{2}$ and, consequently, by employing the time constant of the designed lossless integrator (i.e., $\tau_2 = 1.59$ μs), the time constant of the lossy integrator will be $\tau_1 = 0.795$ μs. The realized pole frequency is $f_0 = 141.6$ kHz, and this is the cut-off frequency of the LPF and the peak (center) frequency of the BPF. Both filters have a maximum gain equal to 0 dB, and the bandwidth of the BPF is $BW = 200$ kHz.

Considering equal transconductances of the transistors in the output branches of both stages with a value of 10.35 μs, then the calculated values of C_1 and C_2 are 8.23 pF and 16.46 pF, respectively.

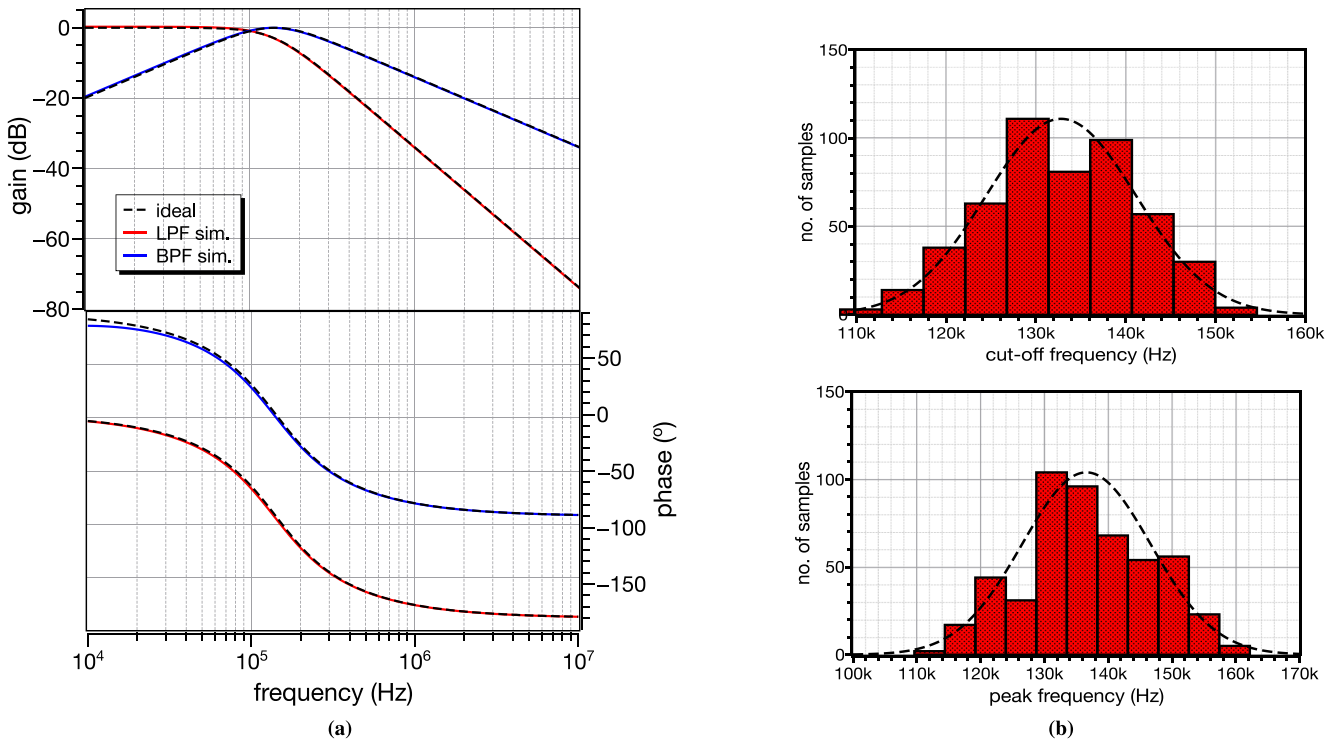


FIGURE 7 | Post-layout simulation results of (a) the gain and phase responses of the LPF and BPF and (b) the Monte Carlo analysis results about the cut-off frequency of the LPF (top) and the center frequency of the BPF (bottom).

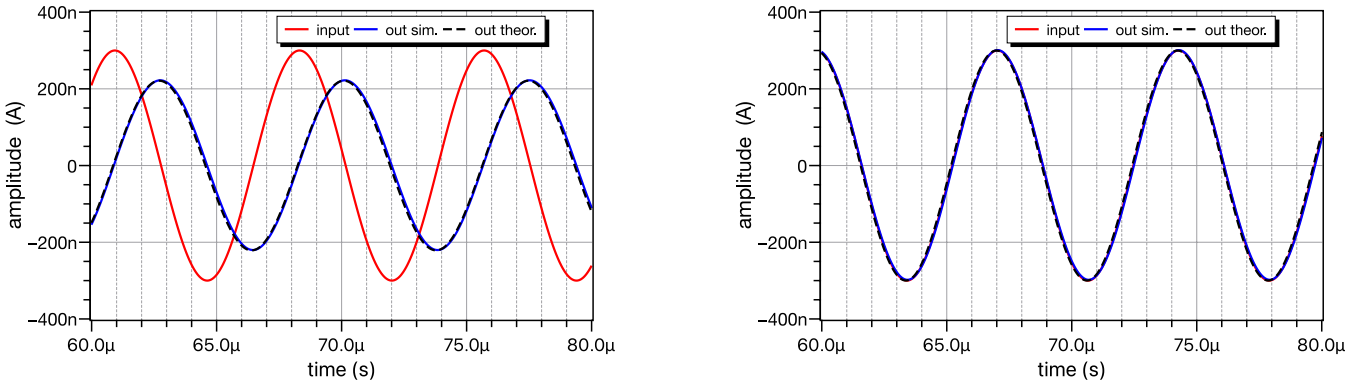


FIGURE 8 | Time-domain simulation results of the (a) LPF stimulated at its cut-off frequency and (b) BPF stimulated at its center frequency.

The layout design of the filter in Figure 5 is demonstrated in Figure 6, where the dimensions are 189.1 µm × 219.45 µm.

The obtained post-layout gain and phase responses of the LPF and BPF are depicted in Figure 7a. With regards to the LPF, the simulated value of the cut-off frequency is 135.4 kHz. The peak of the gain of the BPF is equal to 0 dB, and it is observed at 138 kHz, while the simulated value of the BW of the BPF is 197.5 kHz.

The sensitivity performance of both outputs of the system is evaluated by considering the changes of the cut-off frequency of the LPF as well as of the peak frequency of the BPF. The resulting histograms of the Monte Carlo analysis are demonstrated in Figure 7b, with the values of the standard deviation being 8.4 kHz and 10 kHz, respectively. Comparing them with the corresponding nominal values it is derived that the designed system has reasonable sensitivity characteristics.

The time-domain behavior of the filters is evaluated by stimulating the system with a 0.6 µA peak-to-peak sinusoidal signal at its pole frequency. The derived output waveforms are demonstrated in Figure 8, where the obtained values of the gain and phase difference are −3 dB and −86° for the LPF and 0 dB and 0° for the BPF, confirming their correct behavior in the time-domain.

In addition, the linear performance of the LPF is evaluated through a 10 kHz and variable amplitude stimulus. The Total Harmonic Distortion (THD) becomes equal to 1% for an input signal with *rms* value $i_{in,rms} = 0.21\,\mu A$. Integrating the noise over the pass-band of the LPF, the resulting *rms* value of the input-referred noise is $i_{in,noise,rms} = 1.12nA$; consequently, the predicted value of the dynamic range (DR) of the filter, calculated through the formula: $DR = 20\log(i_{in,rms}/i_{in,noise,rms})$, is 45.5 dB. The power dissipation of the system is 146.1 µW.

4 | Conclusions

The utilization of the introduced lossless integrator for designing current-mode filters leads to more economical solutions than those derived by employing the conventional design, where the lossless integration stage is realized using an extra output branch and an extra current-mirror. This is because the simple lossy integrator stage is reconfigured in such a way that only one DC current source is added. The provided post-layout simulation results validate the proposed concept and the derived frequency and time-domain results are very promising, making this stage an attractive candidate for implementing simple high performance analog signal processing systems. Future research steps include the utilization of the proposed integrator stage in various applications, such as the realization of oscillators, biomedical signal processing systems, and in control systems.

Acknowledgments

The research work was supported by the Hellenic Foundation for Research and Innovation (HFRI) under the 5th Call for HFRI PhD Fellowships (Fellowship Number: 19286). The publication of the article in OA mode was financially supported by HEAL-Link.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

References

1. J. Ramirez-Angulo, M. Róbinson, and E. Sanchez-Sinecio, "Current-Mode Continuous-Time Filters: Two Design Approaches," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 39, no. 6 (1992): 337–341, https://doi.org/10.1109/82.145290.

2. S.-S. Lee, R. H. Zele, D. J. Allstot, and G. Liang, "CMOS Continuous-Time Current-Mode Filters for High-Frequency Applications," *IEEE Journal of Solid-State Circuits* 28, no. 3 (1993): 323–329, https://doi.org/10.1109/4.209999.

3. G. Souliotis, A. Chrisanthopoulos, and I. Haritantis, "Current Differential Amplifiers: New Circuits and Applications," *International Journal of Circuit Theory and Applications* 29, no. 6 (2001): 553–574, https://doi.org/10.1002/cta.171.

4. G. Souliotis and C. Psychalinos, "Harmonic Oscillators Realized Using Current Amplifiers and Grounded Capacitors," *International Journal of Circuit Theory and Applications* 35, no. 2 (2007): 165–173, https://doi.org/10.1002/cta.386.

5. G. Souliotis and I. Haritantis, "Current-Mode Filters Based on Current Mirror Arrays," *International Journal of Circuit Theory and Applications* 36, no. 2 (2008): 173–183, https://doi.org/10.1002/cta.419.

6. C. Wang and R. Zhao, "Continuous-Time Current-Mode Current Mirror Band Pass Filters With Improved Leap-Frog Structure," in *2008 Congress on Image and Signal Processing* (Sanya, China: IEEE, 2008), 146–148.

7. G. Souliotis, "A Current-Mode Automatic Frequency Tuning System for Filters With Current Mirrors," *International Journal of Circuit Theory and Applications* 38, no. 6 (2010): 591–606, https://doi.org/10.1002/cta.589.

8. C. Laoudias and C. Psychalinos, "1.5-V Complex Filters Using Current Mirrors," *IEEE Transactions on Circuits and Systems II: Express Briefs* 58, no. 9 (2011): 575–579, https://doi.org/10.1109/tcsii.2011.21611.

9. C. Laoudias and C. Psychalinos, "Universal Biquad Filter Topology Using Low-Voltage Current Mirrors," *International Journal of Circuit Theory and Applications* 40, no. 1 (2012): 65–75, https://doi.org/10.1002/cta.706.

10. G. Tsirimokou and C. Psychalinos, "Ultra-Low Voltage Fractional-Order Circuits Using Current Mirrors," *International Journal of Circuit Theory and Applications* 44, no. 1 (2016): 109–126, https://doi.org/10.1002/cta.2066.

11. G. Tsirimokou, C. Psychalinos, A. Elwakil, and B. Maundy, "Fractional-Order Multiphase Sinusoidal Oscillator Design Using Current-Mirrors," in *2018 41st International Conference on Telecommunications and Signal Processing (TSP)* (Athens, Greece: IEEE, 2018), 1–4.

12. A. Shrivastava, R. Pandey, and C. Jindal, "Low-Voltage Flipped Voltage Follower Cell Based Current Mirrors for High Frequency Applications," *Wireless Personal Communications* 111 (2020): 143–161, https://doi.org/10.1007/s11277-019-06849-2.

13. Pritty and M. Jhamb, "High-Performance Current Mirror-Based Voltage-Controlled Oscillator for Implantable Devices," in *Micro and Nanoelectronics Devices, Circuits and Systems: Select Proceedings of MNDCS 2021* (Springer, 2021), 339–350.

14. A. Kumar, S. L. Tripathi, C. Verma, M. S. Raboaca, F. M. Enescu, and T. C. Mihaltan, "Design and Analysis of Low Power Bio-Amplifier With Current Mirror Topology at CMOS 45 nm Technology Node," in *2022 14th International Conference on Electronics, Computers and Artificial Intelligence (ECAI)* (Ploiesti, Romania: IEEE, 2022), 1–5.

15. J. Huang, C. Wang, T. Zhou, W. Lu, Y. Zhao, Y. Liu, et al., "A Shifting Current Mirror Driver Circuit for Electrical Impedance Tomography Applications," *IEEE Transactions on Circuits and Systems II: Express Briefs* 70, no. 10 (2023): 3832–3836, https://doi.org/10.1109/tcsii.2023.3288909.

16. K. Nam, G. Choi, M. Yoo, S. Kang, B. Jin, H. Son, et al., "A Low-Noise and Mismatch-Tolerant Current-Mirror-Based Potentiostat Circuit for Glucose Monitoring," *Microelectronics Journal* 132 (2023): 105694, https://doi.org/10.1016/j.mejo.2023.105694.

17. M. Kumngern, F. Khateb, and T. Kulej, "A Novel Multiple-Input Single-Output Current-Mode Shadow Filter and Shadow Oscillator Using Current-Controlled Current Conveyors," *Circuits, Systems, and Signal Processing* 43 (2024): 5438–5462, https://doi.org/10.1007/s00034-024-02729-8.

18. M. Cheng, L. Yang, Z. Ding, S. Li, and J. Lei, "An Improved Memristive Current Mirror Circuit for Continuous Adjustable Current Output," *AEU-International Journal of Electronics and Communications* 170 (2023): 154765, https://doi.org/10.1016/j.aeue.2023.154765.

19. C. Koliopoulos and C. Psychalinos, "A Comparative Study of the Performance of the Flipped Voltage Follower Based Low-Voltage Current Mirrors," in *2007 International Symposium on Signals, Circuits and Systems* (Iasi, Romania: IEEE, 2007), 192–195.

20. A. Zeki and A. Toker, "Tunable Linear CMOS Current Mirror," *Analog Integrated Circuits and Signal Processing* 50 (2007): 261–269, https://doi.org/10.1007/s10470-007-9030-3.

21. M. Gupta, P. Aggarwal, P. Singh, and N. K. Jindal, "Low Voltage Current Mirrors With Enhanced Bandwidth," *Analog Integrated Circuits and Signal Processing* 59 (2009): 97–103, https://doi.org/10.1007/s10470-008-9241-2.

22. B. Aggarwal, M. Gupta, and A. K. Gupta, "A Comparative Study of Various Current Mirror Configurations: Topologies and Characteristics," *Microelectronics Journal* 53 (2016): 134–155, https://doi.org/10.1016/j.mejo.2016.04.015.

23. M. Doreyatim, M. Akbari, M. Nazari, and S. Mahani, "A Low-Voltage Gain Boosting-Based Current Mirror With High Input/Output Dynamic Range," *Microelectronics Journal* 90 (2019): 88–95, https://doi.org/10.1016/j.mejo.2019.05.022.

24. Monika and P. Mittal, "Performance Comparison of FINFET-Based Different Current Mirror Topologies," in *International Conference on Vlsi, Communication and Signal Processing* (Singapore: Springer, 2020), 807–814.

25. K. Monfaredi and H. Faraji Baghtash, "An Extremely Low-Voltage and High-Compliance Current Mirror," *Circuits, Systems, and Signal Processing* 39, no. 1 (2020): 30–53, https://doi.org/10.1007/s00034-019-01175-1.

26. C. Jindal and R. Pandey, "A High Output Resistance, Wide Bandwidth, and Low Input Resistance Current Mirror Using Flipped Voltage Follower Cell," *International Journal of Circuit Theory and Applications* 49, no. 10 (2021): 3286–3301, https://doi.org/10.1002/cta.3085.

27. B. Aggarwal, "Novel Current Mirrors Based on Folded Flipped Voltage Follower Configuration," *Wireless Personal Communications* 123, no. 1 (2022): 645–653, https://doi.org/10.1007/s11277-021-09150-3.