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ABSTRACT

In this paper, two new general topologies for realizing voltage-mode (VM)/current-mode (CM) first-order all-pass filter transfer functions (TFs) are presented. The proposed topologies use single dual-X second-generation current conveyor (DXCCII) and three impedances Z_1, Z_2 and Z_3. Based on the selection of Z_1, Z_2 and Z_3, new VM and CM all-pass filters with unity or variable gains are obtained. The proposed VM/CM filters have high-input/high-output impedances which provide easy cascading at their input/output terminals, respectively. Non-ideal gain and parasitic impedance effects, associated with actual DXCCII implementation, on the performance of the developed topologies are also included. Finally, simulation program with integrated circuit emphasis (SPICE) simulation results based on level 49, 0.25 µm TSMC complementary metal-oxide-semiconductor (CMOS) technology parameters are given to confirm the theory.

Keywords:
All-pass filter, CMOS, Current-mode, Dual-X second-generation current conveyor, Variable gain, Voltage-mode.

1. INTRODUCTION

The dual-X second-generation current conveyor (DXCCII) is a versatile active element which can be used for implementing either voltage-mode (VM) or current-mode (CM) functions [1,2]. Some applications of the DXCCII, such as VM and CM second-order multifunction filters, oscillator and gyrator, have been reported in [1-4]. However, to the best knowledge of the authors no DXCCII-based realization of the first-order all-pass filter has been proposed so far.

All-pass filters find wide applications in analog signal processing to shift phase of the signal while keeping its amplitude constant over the frequency range. In addition, they can be used to equalize the undesired phase change as a result of processing the signal. It is well known that a topology consisting of only grounded passive elements is advantageous from integrated circuit (IC) realization point of view [5-7].

Although operational amplifiers (op-amps) and passive elements can be used to construct all-pass filters [8,9], they suffer from the limited gain–bandwidth product of the op-amp. Fortunately, realization of the first-order all-pass filters using current conveyors (CCs) has received considerable attention in the technical literature [10-33]. The advantages and drawbacks of these first-order all-pass filters can be summarized as follows.

The proposed VM circuits in [10] use single, positive-type, second-generation current conveyor (CCII+) and three to five passive elements but they do not guarantee high input impedance. Higashimura and Fukui proposed VM and CM all-pass filters, respectively, in [11] and [12], employing single, negative-type, second-generation current conveyor (CCII–). Although the proposed filters in [11] and [12] offer high input and high output impedances, respectively, they suffer from employing floating capacitors as well as resistor matching requirement and unity gain. In [13] new CM/VM all-pass filters using single CCII+/CCII–, four resistors and single grounded capacitor were proposed. These filters have high input/high output impedances in VM/CM operations, but they suffer from a constant gain of 0.5. The CC-based VM filters proposed in [14-17] use a floating capacitor and have frequency-dependent input impedances. The first-order all-pass filter given in [18] which employs a third-generation current conveyor (CCIII) operates in transadmittance mode (TAM) (i.e. input as voltage and output as current) and does not offer high input impedance. Also, very simple VM first-order all-pass filters using one differential difference current conveyor (DDCC), one grounded capacitor and one floating resistor were presented in [19] and [20], but their input impedances depend on the values of the employed passive elements. Similarly, a single DDCC-based all-pass filter with a floating capacitor and grounded resistor was presented in [21]. However, the input impedance of this circuit is also frequency-dependent. Recently, two

new VM all-pass filter using single dual-output current conveyors (DO-CCIIs) and single modified negative type current conveyor (MCCII-) were reported in [22] and [23], respectively. These circuits provide high input impedance and employ one grounded capacitor but two floating resistors.

The CM and VM all-pass filters in [24] and [25] employ two CCIIs and four grounded passive elements. The VM filters in [26-28] use only grounded passive elements but require two differential voltage current conveyors (DVCC), and the CM circuit in [29] requires two CCIIs and employs a floating capacitor. The CM all-pass filters in [30] employ single DVCC together with three passive elements but they do not provide gain and employ at least one floating passive element. The CM all-pass circuit with high output impedance reported in [31,32] employs single active element but requires two identical input currents. Thus, an additional active element should be used to provide these identical input currents. Another CM all-pass filter reported in [33] provides low-input and high-output impedances and uses only grounded passive elements, but requires two DO-CCIIs as active elements. Finally, a new CM all-pass filter based on an active element, namely, Z-copy current inverter transconductance amplifier (ZC-CITA), and only one grounded capacitor was reported in [34]. The ZC-CITA is composed of a dual-output operational transconductance amplifier (OTA), a current mirror and a current inverter circuit.

In this paper, novel VM and CM first-order all-pass filters using a single DXCCII and four passive components, (grounded capacitor(s) and grounded or floating resistors), are proposed. The proposed all-pass filters possess attractive features such as using single active component, low sensitivities, variable gain (some of them), use of only grounded capacitor(s) and high input impedance (high output impedance) for VM (CM) realizations. Non-ideal gain and parasitic impedance effects of the DXCCII on the transfer functions (TFs) of the proposed filters are investigated.

2. DXCCII AND PROPOSED CIRCUITS

The DXCCII, whose symbol is shown in Figure 1, is an active element ideally defined with following voltage–current terminal relationships:

$$I_Y = 0,\ I_{Zp} = I_{Xp},\ I_{Zn} = I_{Xn},\ V_{Xp} = V_Y,\ V_{Xn} = -V_Y \tag{1}$$

However, including its non-ideal voltage and current gains as well as parasitic impedance effects, the DXCCII can be characterized by the following matrix equation:

$$\begin{bmatrix} I_Y \\ I_{Zp} \\ I_{Zn} \\ V_{Xp} \\ V_{Xn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & sC_y + \frac{1}{R_y} & 0 & 0 \\ \alpha_1(s) & 0 & 0 & sC_{zp} + \frac{1}{R_{zp}} & 0 \\ 0 & \alpha_2(s) & 0 & 0 & sC_{zn} + \frac{1}{R_{zn}} \\ Z_{xp}(s) & 0 & \beta_1(s) & 0 & 0 \\ 0 & Z_{xn}(s) & -\beta_2(s) & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{Xp} \\ I_{Xn} \\ V_Y \\ V_{Zp} \\ V_{Zn} \end{bmatrix} \tag{2}$$

Here, $\alpha_i(s) = \alpha_{oi}/(1 + s/\omega_{\alpha i})$ and $\beta_i(s) = \beta_{oi}/(1 + s/\omega_{\beta i})$ ($i = 1, 2$) are the frequency-dependent non-ideal current gains and voltage gains, respectively. The DC non-ideal gains, α_{oi} and β_{oi}, are ideally equal to unity and their bandwidths, $\omega_{\alpha i}$ and $\omega_{\beta i}$, are ideally equal to infinity. It is obvious that the *Z*- and *Y*-terminal parasitic resistors (R_z, R_y) and capacitors (C_z, C_y) are ideally equal to infinity and zero, respectively. The *X*-terminal parasitic impedance $Z_x(s) = R_x + sL_x$ is ideally equal to zero where R_x and L_x are called the *X*-terminal parasitic resistor and inductor, respectively.

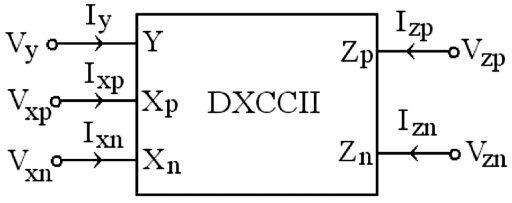

Figure 1: Symbolic representation of the DXCCII.

The proposed configurations for realizing VM and CM all-pass filters are shown in Figures 2 and 3, respectively. Assuming ideal DXCCII, routine analysis of the circuits in Figures 2 and 3 gives the following TF:

$$\frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} = Z_3 \frac{Z_2 - Z_1}{Z_1 Z_2} \tag{3}$$

2.1 VM First-order All-pass Filters

Selecting different impedances for Z_1, Z_2 and Z_3 in Figure 2, one can obtain two VM all-pass filters as follows.

a) VM circuit 1: If $Z_1 = R$, $Z_2 = 1/(sC)$ and $Z_3 = (R) \| 1/(sC)$ are chosen, a unity-gain, non-inverting, all-pass with following TF is obtained.

$$\frac{V_{out}}{V_{in}} = \frac{1 - sCR}{1 + sCR} \tag{4}$$

The filter in frequency domain has the following phase response in ideal case:

$$\phi(\omega) = -2\tan^{-1}(\omega CR) \tag{5}$$

Note that by interchanging the resistor and capacitor at terminals X_p and X_n, a unity-gain inverting all-pass filter can be obtained as

$$\frac{V_{out}}{V_{in}} = -\frac{1-sCR}{1+sCR} \tag{6}$$

which has a phase response in frequency domain as

$$\phi(\omega) = 180^0 - 2\tan^{-1}(\omega CR) \tag{7}$$

The proposed VM circuits have the advantage of using only grounded passive elements, which is a desired feature in integrated circuit (IC) implementation.

b) VM circuit 2: If $Z_1 = R_1$, $Z_2 = R_2 + 1/(sC)$ and $Z_3 = R_3$ are chosen, the TF in Equation (3) becomes

$$\frac{V_{out}}{V_{in}} = \frac{R_3}{R_1}\cdot\frac{1-sC(R_1-R_2)}{1+sCR_2} \tag{8}$$

Selecting $R_1 = 2R_2$ results in a gain-variable non-inverting first-order all-pass filter as:

$$\frac{V_{out}}{V_{in}} = \frac{R_3}{R_1}\cdot\frac{1-sCR_2}{1+sCR_2} \tag{9}$$

Therefore the phase response of the filter in frequency domain can be given by

$$\phi(\omega) = -2\tan^{-1}(\omega CR_2) \tag{10}$$

Note that by selecting $Z_1 = R_1 + 1/(sC)$, $Z_2 = R_2$ and $Z_3 = R_3$ with $R_2 = 2R_1$, a gain-variable inverting all-pass filter with following TF and phase response in frequency domain can be obtained:

$$\frac{V_{out}}{V_{in}} = -\frac{R_3}{R_2}\cdot\frac{1-sCR_1}{1+sCR_1} \tag{11}$$

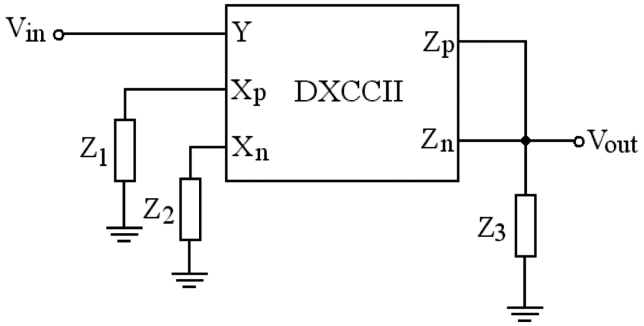

Figure 2: Proposed VM circuit using a single DXCCII.

$$\phi(\omega) = 180 - 2\tan^{-1}(\omega CR_1) \tag{12}$$

It should be mentioned that the gain of the filters with TFs in Equations (9) and (11) can be controlled by changing R_3, without disturbing their phase responses.

2.2 CM First-order All-pass Filters

Similar to the VM filters discussed in Section 2.1, selecting different impedances for Z_1, Z_2 and Z_3 in the circuit of Figure 3 results in CM all-pass filters as follows.

a) CM circuit 1: If $Z_1 = R$, $Z_2 = 1/(sC)$ and $Z_3 = R \parallel 1/(sC)$ are chosen, the following CM TF is found.

$$\frac{I_{out}}{I_{in}} = \frac{1-sCR}{1+sCR} \tag{13}$$

Therefore, a unity-gain non-inverting all-pass filter is obtained. Note that by interchanging the resistor and capacitor at terminals X_p and X_n, an inverting all-pass filter with unity gain is obtained as

$$\frac{I_{out}}{I_{in}} = -\frac{1-sCR}{1+sCR} \tag{14}$$

The phase responses of the TFs in Equations (13) and (14) are same as given in Equations (5) and (7), respectively. As mentioned for the VM circuit 1, the proposed CM filter uses only grounded passive elements, thus making it attractive from IC implementation point of view.

b) CM circuit 2: If $Z_1 = R_1$, $Z_2 = R_2 + 1/(sC)$, and $Z_3 = R_3$ are chosen, a non-inverting, gain-variable filter with the following CM TF is obtained:

$$\frac{I_{out}}{I_{in}} = \frac{R_3}{R_1}\cdot\frac{1-sC(R_1-R_2)}{1+sCR_2} \tag{15}$$

Selecting $R_1 = 2R_2$ results in a first-order CM all-pass filter TF as:

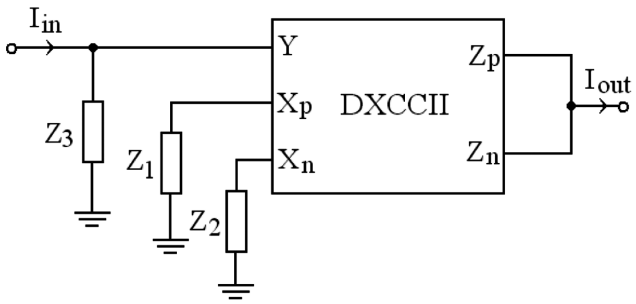

Figure 3: Proposed CM circuit using a single DXCCII.

$$\frac{I_{out}}{I_{in}} = \frac{R_3}{R_1} \cdot \frac{1 - sCR_2}{1 + sCR_2} \tag{16}$$

Note that by selecting $Z_1 = R_1 + 1/(sC)$, $Z_2 = R_2$ and $Z_3 = R_3$ with $R_2 = 2R_1$, an inverting, gain-variable, all-pass filter is obtained as

$$\frac{I_{out}}{I_{in}} = -\frac{R_3}{R_2} \cdot \frac{1 - sCR_1}{1 + sCR_1} \tag{17}$$

The phase responses of the TFs in Equations (16) and (17) are the same as given in Equations (10) and (12), respectively. Hence, the gain of these CM filters can be controlled by changing R_3 without disturbing their relevant phase responses. Finally, it should be mentioned that the grounded and floating resistors of the proposed circuits can be realized using electronically controllable CMOS-based grounded and floating resistors reported in [35] and [36], respectively.

3. NON-IDEALITY AND MISMATCHING EFFECTS

In this section, non-ideality effects of the DXCCII (non-ideal gain and parasitic effects) and mismatching effects of the passive elements on the TF of the proposed all-pass filters are investigated. If non-ideal gains of the DXCCII in the all-pass filters in Figures 2 and 3 are taken into account (i.e. matrix Equation (1) with only non-ideal gains), the TF in Equation (3) becomes

$$\frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} = Z_3 \frac{Z_2\alpha_1(s)\beta_1(s) - Z_1\alpha_2(s)\beta_2(s)}{Z_1 Z_2} \tag{18}$$

As an example, if $Z_1 = R$, $Z_2 = 1/(sC)$ and $Z_3 = R \parallel 1/(sC)$ are chosen for the TF in Equation (18), the following TF is realized:

$$\frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} = \frac{\alpha_1(s)\beta_1(s) - sCR\alpha_2(s)\beta_2(s)}{1 + sCR} \tag{19}$$

It is seen from Equation (19) that non-ideal gains are in the form of multipliers. Thus, at sufficiently low frequencies $f << \min\{\omega_{\alpha i}, \omega_{\beta i}\}/(2\pi)$ $(i = 1, 2)$, $\alpha_{o1}\beta_{o1} = \alpha_{o2}\beta_{o2} = k$ can be achieved if tuning techniques of electronically tunable current conveyors (ECCIIs) [37] or voltage/current gain variable current conveyors (VCG-CCII) [38] are used in the implementation of the DXCCII. On the other hand, considering only parasitic impedances of the DXCCII (i.e. matrix Equation (1) with only parasitic impedances) the TFs of the all-pass filters depicted in Figures 2 and 3 are computed, respectively, as

$$\frac{V_{out}}{V_{in}} = \left(Z_3 \left\| R_{zp} \right\| R_{zn} \left\| \frac{1}{sC_{zn}} \right\| \frac{1}{sC_{zp}} \right) \frac{(Z_2 + Z_{xn}) - (Z_1 + Z_{xp})}{(Z_1 + Z_{xp})(Z_2 + Z_{xn})} \tag{20}$$

$$\frac{I_{out}}{I_{in}} = \left(Z_3 \left\| R_y \right\| \frac{1}{sC_y} \right) \frac{(Z_2 + Z_{xn}) - (Z_1 + Z_{xp})}{(Z_1 + Z_{xp})(Z_2 + Z_{xn})} \tag{21}$$

It is observed from Equations (20) and (21) that only if $Z_1 = R$, $Z_2 = 1/(sC)$ and $Z_3 = R \parallel 1/(sC)$ are chosen for the circuits in Figures 2 and 3, the X-terminal parasitic resistor R_{xn} along with the capacitor C brings extra poles/zeros to the TFs which can restrict the high frequency operation of the circuit [39]. In fact, the proposed VM and CM circuits of type 2 suffer less from parasitic resistance at X-terminals than the proposed circuits of type 1 because in type 2 circuits, $R + 1/sC$ impedances are connected at X-terminal and hence the resistor can be floating followed by a grounded capacitor and in this case, the parasitic resistance at X-terminal can be easily absorbed by added physical resistor and by making good characterization for the designed DXCCII. The low frequency performances of the proposed circuits are not affected from the parasitic impedances, since there is no single grounded capacitor connected to the Z terminals in the proposed VM or CM filters [7]. Finally, if unmatched capacitors and resistors are selected in Equation (18) as $Z_1 = R_1$, $Z_2 = 1/(sC_1)$ and $Z_3 = R_2 \parallel 1/(sC_2)$, the following TF is obtained:

$$\frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} = \frac{R_2\alpha_1(s)\beta_1(s)}{R_1} \frac{1 - sC_1R_1 \dfrac{\alpha_2(s)\beta_2(s)}{\alpha_1(s)\beta_1(s)}}{1 + sC_2R_2} \tag{22}$$

It is observed from Equation (22) that for realizing a unity-gain, all-pass filter with a pole frequency of $f_o = 1/(2\pi C_2R_2)$, one should select $C_2 = C_1\alpha_2(s)\beta_2(s)$ and $R_2 = R_1/\{\alpha_1(s)\beta_1(s)\}$, where operating frequency of the proposed all-pass filter is assumed to be much lesser than pole frequencies of non-ideal gains of the DXCCII.

4. SIMULATION RESULTS AND DISCUSSION

Simulation program with integrated circuit emphasis (SPICE) simulation program is used to test the performance of the proposed circuits. The complementary metal-oxide-semiconductor (CMOS) internal structure of the DXCCII used in the simulations is shown in Figure 4 [40] with transistor dimensions given in Table 1. Simulations are based on level 49, 0.25 μm TSMC CMOS technology parameters [41]. The supply voltages and

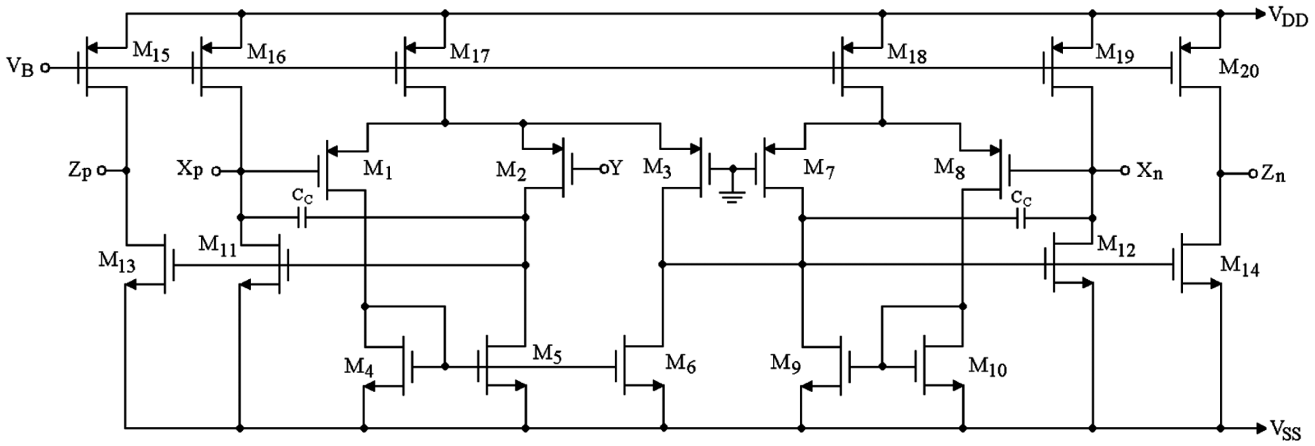

Figure 4: CMOS structure of the DXCCII [40].

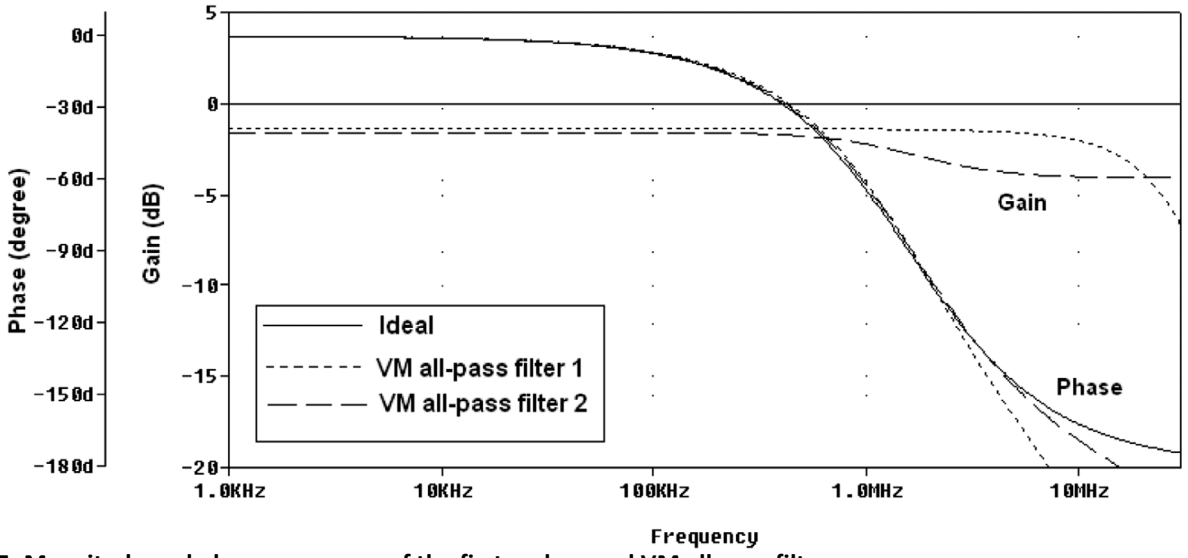

Figure 5: Magnitude and phase responses of the first and second VM all-pass filters.

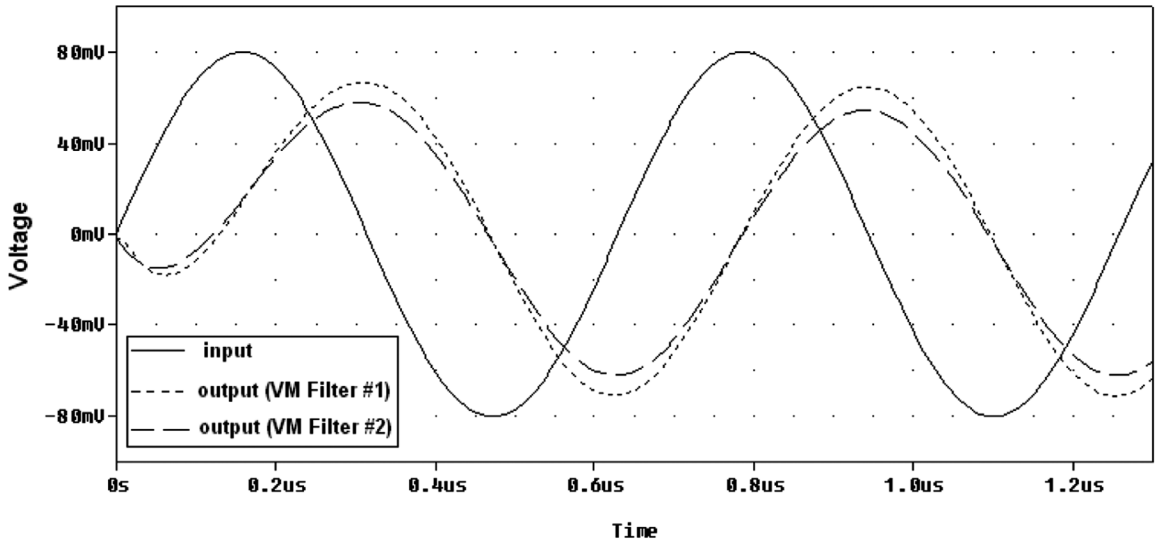

Figure 6: Time-domain responses of the proposed VM all-pass filters.

compensation capacitors are selected as $V_{DD} = -V_{SS} = 1.25$ V, $V_B = -0.3$ V, and $C_{C1} = C_{C2} = 0.6$ pF. The VM all-pass filters with a pole frequency of $f_o = 1.59$ MHz and unity gain are obtained by selecting $R = 1$ kΩ and $C = 0.1$ nF for the first circuit as well as $R_1 = R_3 = 2$ kΩ, $R_2 = 1$ kΩ and $C = 0.1$ nF for the second one.

Both the ideal and simulated phase and magnitude responses of the proposed VM all-pass filters are shown in Figure 5. The output noise and equivalent input noise of the first VM circuit are found to be $2.473 \times 10^{-8}\,\text{V}/\sqrt{\text{Hz}}$ and $2.91 \times 10^{-8}\,\text{V}/\sqrt{\text{Hz}}$, respectively, at frequency of 1.59

Table 1: Aspect ratios of the MOS transistors in Figure 4

MOS transistors	W (μm)/L (μm)
M_1, M_2, M_4, M_5 M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{20}	2/0.25
M_3, M_6, M_7, M_8, M_9, M_{10}	4/0.25
M_{11}, M_{12}, M_{13}, M_{14}	16/0.25

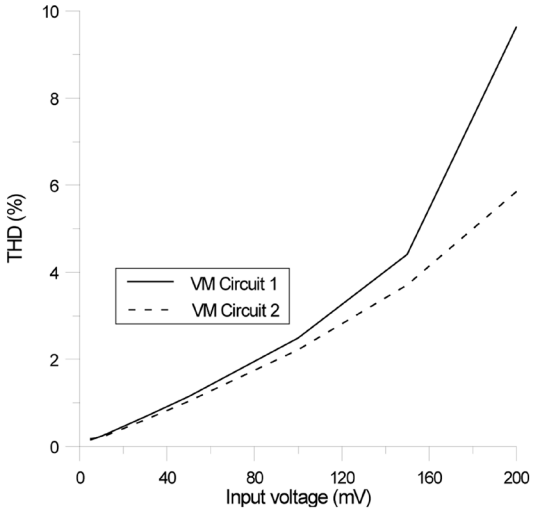

Figure 7: THD variation of the proposed VM all-pass filters against input voltage (peak).

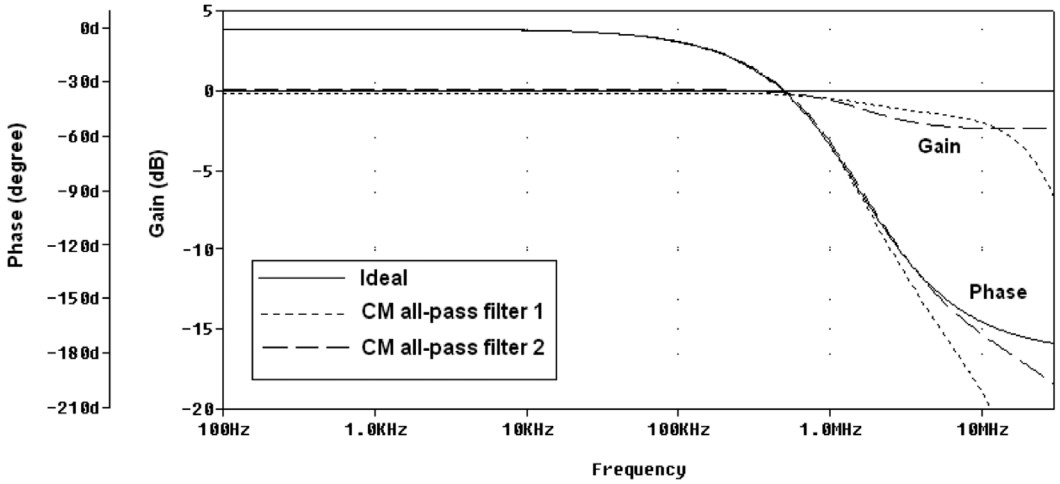

Figure 8: Magnitude and phase responses of the first and second CM all-pass filters.

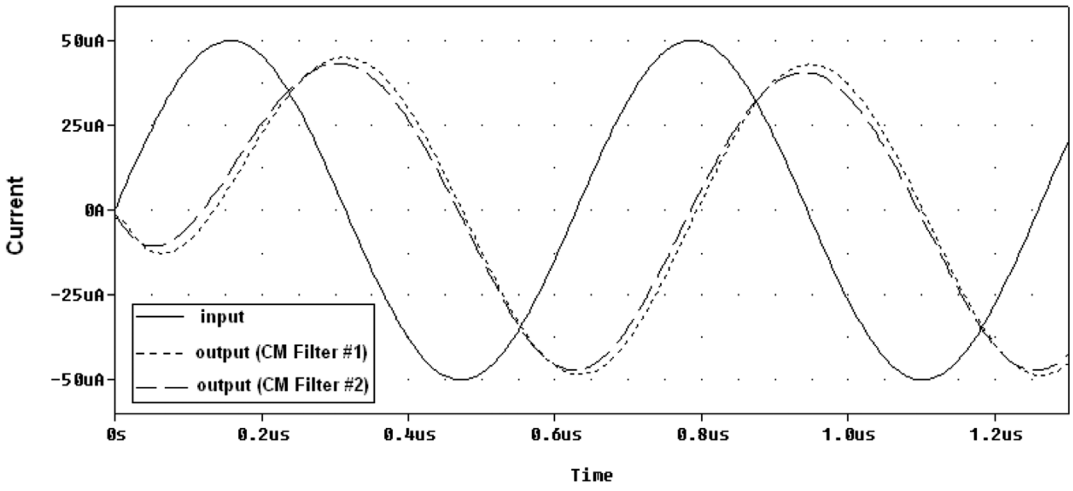

Figure 9: Time-domain responses of the proposed CM all-pass filters.

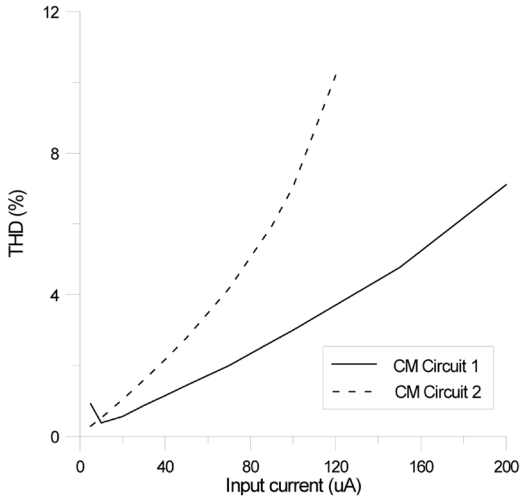

Figure 10: THD variation of the proposed CM all-pass filters against input current (peak).

MHz. The output and equivalent input noise values for the second VM filter are evaluated as 3.824×10^{-8} V/√Hz and 5.246×10^{-8} V/√Hz, respectively. The time-domain responses of the proposed VM filters at 1.59 MHz are shown in Figure 6. The discrepancy between ideal and simulated results can be attributed to the non-ideal gain and parasitic impedance effects of the DXCCII. The variation of the total harmonic distortion (THD) versus applied sinusoidal input voltage for both of the proposed VM all-pass filters at f_o = 1.59 MHz are given in Figure 7. Here, the biasing currents of the differential pairs in the internal structure of the DXCCII shown in Figure 4 (drain currents of transistors M_{17} and M_{18}) are equal to 89.1 μA. Likewise, the biasing currents of the transistor M_{13} (M_{14}) at terminal Z_p (Z_n) and M_{11} (M_{12}) at terminal X_p (X_n) are all equal to 165 μA. From Figure 7 it can be seen that the second VM filter has better THD performance than the first one.

Similarly, CM all-pass filters are simulated for a pole frequency of f_o = 1.59 MHz and unity gain by selecting R = 1 kΩ and C = 0.1 nF for the first circuit as well as $R_1 = R_3$ = 2 kΩ, R_2 = 1 kΩ and C = 0.1 nF for the second one. Both the ideal and simulated phase and magnitude responses of the proposed CM filters are depicted in Figure 8. Comparing Figures 5 and 8 demonstrates that the proposed CM filters have better magnitude responses (almost 0 dB) than proposed VM ones. The output noise and equivalent input noise of the first CM filter with a 1 kΩ resistive load are calculated as 3.29×10^{-8} V/√Hz and 4.127×10^{-11} A/√Hz, respectively, at frequency of 1.59 MHz. For the same conditions, the second CM filter exhibits output and equivalent input noises of 2.037×10^{-8} V/√Hz and 2.661×10^{-11} A/√Hz, respectively. The time-domain responses of the proposed CM filters at 1.59 MHz are shown in Figure 9. The variations of the THD against applied sinusoidal input current for both of the proposed CM all-pass filters at f_o = 1.59 MHz are given in Figure 10, where the biasing currents of the DXCCII are the same as given for the VM filters. It can be seen that the first CM filter exhibits better THD performance than the second one. Moreover, the total power dissipation of the proposed VM and CM circuits are found to be approximately 2.1 mW.

5. CONCLUSION

In this study, novel VM and CM first-order all-pass filters with unity/variable gains employing a single DXCCII are proposed. The developed VM and CM filters have high input impedances and high output impedances, respectively, and use grounded capacitor(s); thus, they are suitable for IC implementation. The non-ideality analyses of the introduced filters are given. The simulation results are in close proximity with the theoretical ones, whereas the discrepancy between them arises from the effects of non-ideal gains and parasitic impedances of the DXCCII.

REFERENCES

1. A Zeki and A Toker, "The dual-X current conveyor (DXCCII): A new active device for tunable continuous- time filters," *International Journal of Electronics*, Vol. 89, pp. 913-23, 2002.
2. A Zeki and A Toker, "DXCCII-based tunable gyrator," *International Journal of Electronics and Communications (AEÜ)*, Vol. 59, pp. 59-62, 2005.
3. E Yuce and S Minaei, "ICCII-based universal current-mode analog filter employing only grounded passive components, *Analog Integrated Circuits and Signal Processing*, Vol. 58, pp. 161-9, 2009.
4. S Minaei, "Electronically tunable current-mode universal biquad filter using dual-X current conveyors" *Journal of Circuits, Systems and Computers*, Vol. 18, pp. 665-80, 2009.
5. G W Roberts and A S Sedra, "All current-mode frequency selective circuits," *Electronics Letters*, Vol. 25, pp. 759-61, 1989.
6. R Senani and V K Singh, "KHN-equivalent biquad using current conveyors," *Electronics Letters*, Vol. 31, pp. 626-28, 1995.
7. E Yuce and S Minaei, "Universal current-mode filters and parasitic impedance effects on the filter performances," *International Journal of Circuit Theory and Applications*, Vol. 36, pp. 161-71, 2008.
8. D T Comer, D J Comer, and J R Gonzales, "A high frequency integrable band pass filter configuration," *IEEE Transactions on Circuits and Systems-II. Analog and Digital Signal Processing*, Vol. 44, pp. 856-61, 1997.
9. S J G Gift, "The application of all-pass filters in the design of multiphase sinusoidal systems," *Microelectronics Journal*, Vol. 31, pp. 9-13, 2000.
10. O Cicekoglu, H Kuntman, and S Berk, "All-pass filters using a single current conveyor," *International Journal of Electronics*, Vol. 86, No. 8, pp. 947-55, 1999.
11. M Higashimura and Y Fukui, "Realization of all-pass networks using a current conveyor," *International Journal of Electronics*, Vol. 65, No. 2, pp. 249-50, 1988.
12. M Higashimura and Y Fukui, "Realization of current mode all-pass networks using a current conveyor," *IEEE Trans*. CAS, Vol. 37, No. 5, pp. 660-1, 1990.
13. A M Soliman, "Generation of current conveyor based all-pass filters from op-amp based circuits," *IEEE Trans*. CAS-II. Vol. 44, No. 4, pp. 324-30, 1997.

14. I A Khan and S Maheshwari, "Simple first order all-pass section using a single CCII," *International Journal of Electronics*, Vol. 87, No. 3, pp. 303-6, 2000.
15. S Maheshwari and I A Khan, "Novel first order all-pass sections using a single CCIII," *International Journal of Electronics*, Vol. 88, No. 7, pp. 773-8, 2001.
16. A Toker, S Ozcan, H Kuntman, and O Cicekoglu, "Supplementary all-pass sections with reduced number of passive elements using a single current conveyor," *International Journal of Electronics*, Vol. 88, No. 9, pp. 969-76, 2001.
17. N Pandey and S K Paul, "All-pass filters based on CCII- and CCCII-," *International Journal of Electronics*, Vol. 91, No. 8, pp. 485-9, 2004.
18. S Minaei, "A new high performance CMOS third generation current conveyor (CCIII) and its application," *Electrical Engineering*, Vol. 85, No. 3, pp. 147-53, 2003.
19. J W Horng, C L Hou, C M Chang, Y T Lin, I C Shiu, and W Y Chiu, "First-order all-pass filter and sinusoidal oscillators using DDCCs," *International Journal of Electronics*, Vol. 93, No. 7, pp. 457-66, 2006.
20. H P Chen and K H Wu, "Grounded-capacitor first-order filter using minimum components," *IEICE Trans. Fundamentals*, Vol. E89-A, No. 12, pp. 3730-1, 2006.
21. M A Ibrahim, H Kuntman, and O Cicekoglu, "First-order all-pass filter canonical in the number of resistors and capacitors employing a single DDCC," *Circuits, Systems, and Signal Processing*, Vol. 22, No. 5, pp. 525-36, 2003.
22. B Metin and K Pal, "Cascadable allpass filter with a single DO-CCII and a grounded capacitor", *Analog Integrated Circuits and Signal Processing*, Vol. 61, pp. 259-63, 2009.
23. B Metin and O Cicekoglu, "Component reduced all-pass filter with a grounded capacitor and high impedance input", *International Journal of Electronics*, Vol. 96, No. 5, pp. 445-55, 2009.
24. J W Horng, L Hou, M Chang, Y Chung, L Liu, and T Lin, "High output impedance current-mode first-order allpass networks with four grounded components and two CCIIs," *International Journal of Electronics*, Vol. 93, No. 9, pp. 613-21, 2006.
25. J W Horng, "Current conveyors based allpass filters and quadrature oscillators employing grounded capacitors and resistors," *Computers and Electrical Engineering*, Vol. 31, No. 1, pp. 81-92, 2005.
26. S Maheshwari, "High input impedance VM-APSs with grounded passive elements," *IET Circuits, Devices and Systems*, Vol. 1, No. 1, pp. 72-8, 2007.
27. S Maheshwari, "High input impedance voltage-mode first-order all-pass sections," *International Journal of Circuit Theory and Applications*, Vol. 36, pp. 511-22, 2008.
28. S Maheshwari, "A canonical voltage-controlled VM-APS with a grounded capacitor," *Circuits Systems and Signal Processing*, Vol. 27, pp. 123-32, 2008.
29. S Maheshwari, "A new current-mode current-controlled all-pass section," *Journal of Circuits, Systems, and Computers*, Vol. 16, pp. 181-9, 2007.
30. S Minaei and S M A Ibrahim, "General configuration for realizing current-mode first-order all-pass filter using DVCC," *International Journal of Electronics*, Vol. 92, No. 6, pp. 347-56, 2005.
31. S Maheshwari, "High output impedance current-mode all-pass sections with two grounded passive components," *IET: Circuits, Devices, and Systems*, Vol. 2, No. 2, pp. 234-42, 2008.
32. S Maheshwari, "Grounded capacitor CM-APS with high output impedance," *Journal of Circuits, Systems and Computers*, Vol. 16, No. 4, pp. 567-76, 2007.
33. B Metin, K Pal, and O Cicekoglu, "All-pass filter for rich cascadability options easy IC implementation and tunability," *International Journal of Electronics*, Vol. 94, No. 11, pp. 1037-45, 2007.
34. D Biolek and V Biolkova, "Allpass filter employing one grounded capacitor and one active element" *Electronics Letters*, Vol. 45, No. 16, pp. 807-8, 2009.
35. G Wilson and P K Chan, "Novel voltage-controlled grounded resistor," *Electronics Letters,* Vol. 25, pp. 1725-6, 1989.
36. G Wilson and P K Chan, "Floating CMOS resistor," *Electronics Letters*, Vol. 29, pp. 306-7, 1993.
37. S Minaei, O K Sayin, and H Kuntman, "A new CMOS electronically tunable current conveyor and its application to current-mode filters," *IEEE Transactions on Circuits and Systems Part-I: Regular Papers*, Vol. 53, pp. 1448-57, 2006.
38. A De Marcellis, G Ferri, N C Guerrini, G Scotti, V Stornelli, and A Trifiletti, "The VCG-CCII: A novel building block and its application to capacitance multiplication," *Analog Integrated Circuits and Signal Processing*, Vol. 58, No. 1, pp. 55-9, 2009.
39. A Fabre, O Saaid, and H Barthelemy, "On the frequency limitations of circuits based on second generation current conveyors", *Analog Integrated Circuits and Signal Processing*, Vol. 7, pp. 113-29, 1995.
40. E Yuce and S Minaei "A new full-wave rectifier circuit employing single dual-X current conveyor" *International Journal of Electronics*, Vol. 95, No. 8, pp. 777-84, 2008.
41. E Yuce, S Minaei, and O Cicekoglu, "Full-wave rectifier realization using only two CCII+s and NMOS transistors", *International Journal of Electronics,* Vol. 93, No. 8, pp. 533-41, 2006.

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