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A novel full-wave rectifier/sinusoidal frequency doubler topology based on CFOAs

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Abstract A novel topology for realizing voltage-mode (VM) full-wave rectifier/sinusoidal frequency doubler based on current feedback operational amplifiers (CFOAs) and n-channel metal-oxide semiconductor (NMOS) transistors is proposed in this study. The proposed full-wave rectifier structure employs two CFOAs and three enhancement-mode NMOS transistors. With a slight modification, the sinusoidal frequency doubler circuit can be adopted from the full-wave rectifier circuit by replacing a grounded resistor instead of one of the NMOS transistors. Both of the proposed circuits enjoy low output and high input impedance properties which make them convenient for cascading easily with other VM circuits without needing any extra buffer circuits. No passive component matching conditions are needed. The proposed circuits are simulated by using SPICE program to verify the theoretical analysis.

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Keywords Full-wave rectifier · Frequency doubler · CFOA · NMOS transistors · Low output and high input impedances

1 Introduction

In many instrumentation, measurement and communication circuits, such as AC voltmeters, ammeters and wattmeters, piecewise linear function generators, RF demodulators, various nonlinear analogue signal-processors, signal-polarity detectors, averaging circuits and peak-value detectors, rectifier circuits and sinusoidal frequency doublers are used as basic building blocks [1, 2]. Because of the limitations of the diode threshold voltages which are about 0.7 V for silicon diodes and 0.3 V for germanium diodes, it is not possible to use diode-only rectifiers for low-voltage high-precision applications. Therefore, operational amplifier (op-amp) based precision full-wave rectifiers, such as the one given in Fig. 1 [1], were developed before. If $V_{in} > 0$ in the full-wave rectifier of Fig. 1, D_1 is ON, D_2 is OFF and $V_{out} = V_{in}$. Similarly, if $R_2 = R_1$ and $V_{in} < 0$ in the full-wave rectifier of Fig. 1, D_1 is OFF, D_2 is ON and $V_{out} = -V_{in}$. In other words, $V_{out} = |V_{in}|$.

By the usage of the op-amps, the threshold voltage restrictions of the p–n junction diodes are overcome, which result in an achievement of a full-wave rectification of low-level signals. Nevertheless, disadvantage of the finite small signal dV/dt (slew rate) of the op-amps causes a crucial distortion in signal of the full-wave rectifier. Also, even the use of the high slew rate op-amps does not solve this problem because of a small-signal transient problem [2]. Hence, precision rectifiers employing other active elements, especially those based on current signals, have to be presented. Probably, these types of rectifiers can be

operated at high frequencies since it is suitable to drive the diodes by currents instead of voltages.

Normally, a frequency doubling circuit can be implemented using an analogue multiplier [3, 4] or a translinear cell using bipolar junction transistors [5–7]. Surakampontorn et al. [8] showed in 1988 a circuit principle that can be employed to realize both a sinusoidal frequency doubler and a full-wave rectifier.

For a full-wave rectifier, a number of full-wave rectifier structures including various active components have been presented in the related open literature [2, 9–25]. However, a few numbers of circuits that can realize both the full-wave rectifier and sinusoidal frequency doubler have been reported [8, 23, 26–28] in the literature.

A novel topology for realizing both a full-wave rectifier and a sinusoidal frequency doubler working in voltage-mode (VM) is proposed in this work. The full-wave rectifier circuit employs two current feedback operational amplifiers (CFOAs) and three enhancement-mode n-channel metal-oxide semiconductor (NMOS) transistors while the frequency doubler circuit, adopted from the rectifier circuit, employs two CFOAs, two NMOS transistors and one grounded resistor. Both of the proposed circuits possess low output and high input impedances required for direct cascading with other VM configurations. Thus, additional buffer circuits are not needed. No passive component matching conditions for both of the proposed circuits are required. SPICE simulation results are given to confirm the validity of the theoretical analysis of the proposed circuits. In order to show the superiority of the proposed topology, a comparison table is given in Table 1 in which the proposed circuit and previously published ones are compared.

2 The proposed full-wave rectifier/sinusoidal frequency doubler topology

The CFOA, whose electrical symbol depicted in Fig. 2, is a four-terminal active device which can be defined by the following terminal equations:

$$I_Y = 0 \tag{1a}$$

$$V_X = V_Y \tag{1b}$$

$$I_Z = I_X \tag{1c}$$

$$V_W = V_Z \tag{1d}$$

From Eqs. (1), it can be seen that the terminals Y and Z have high impedances as well as terminals X and W possess low impedances. The voltage at terminal X follows the voltage at the Y terminal i.e., acts as a voltage-controlled voltage source. Moreover, the current at the Z terminal follows the current of the X terminal in the same direction, i.e., acts as a current controlled current source and the voltage at the W terminal follows the voltage at the Z terminal, i.e., acts as a voltage buffer.

The proposed full-wave rectifier structure containing two CFOAs and three NMOS transistors is depicted in Fig. 3. All the three NMOS transistors of the proposed rectifier structure are diode-connected. If the input signal of the proposed full-wave rectifier is in positive cycle ($V_{in}(t)_+$), the input voltage which is conveyed from terminal Y of the second CFOA to its terminal X can produce a current passing through the NMOS transistor M_B. Further, according to the terminal relationship of the CFOA given in Eqs. (1), a current with same direction can pass through M_C. It is assumed that $V_{B1} = V_{Tn}$, and $V_{B2} = V_{B3} = -V_{Tn}$, the current passing through M_B can be given as:

$$I_{DB} = \frac{k_n}{2}\left(V_{in}(t)_+ + V_{Tn} - V_{Tn}\right)^2 = \frac{k_n}{2}\left(V_{in}(t)_+\right)^2 \tag{2}$$

where V_{Tn} is the threshold voltage and k_n is the gain factor of the NMOS transistor. Accordingly, considering identical V_{Tn} and k_n for all the three NMOS transistors, the current passing through NMOS transistor M_C can be given as:

$$I_{DC} = \frac{k_n}{2}\left(V_o(t) + V_{Tn} - V_{Tn}\right)^2 = \frac{k_n}{2}\left(V_o(t)\right)^2 \tag{3}$$

Since

$$I_{DC} = I_{DB} \tag{4}$$

Therefore

$$V_o(t) = V_{in}(t)_+ \tag{5}$$

Therefore, the positive cycle signal is passed to the output. Likewise, if the input is in negative cycle ($V_{in}(t)_-$), the input voltage is conveyed from the terminal Y of the second CFOA to its terminal X and then to the terminal Y.

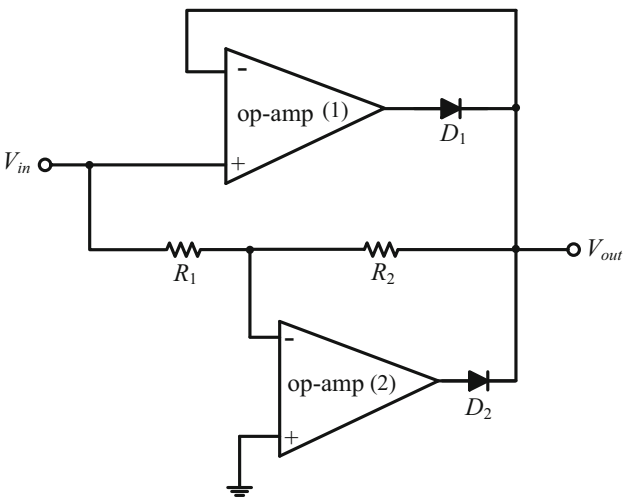

Fig. 1 A conventional full-wave rectifier [1]

Table 1 Comparison of the proposed VM topology with previously published ones

References	Low output impedance	High input impedance	No. of active elements	No. of resistors	No. of grounded resistors	No. of transistors	Power dissipation (mW)	Both rectifier and frequency doubler
[2]	No	Yes	1 CCII+ Current mirrors	2	2	18 + 18	NA	No
[8]—1st	No	No	6 Current mirrors	2	2	24	NA	Yes
[8]—2nd	No	Yes	1 Translinear loop 3 Current mirrors	2	2	17	NA	Yes
[9]	No	Yes	2 CCII	2	1	2*18	NA	No
[10]	No	Yes	1 DO–OTA	1	1	24	NA	No
[11]	No	No	2 CCII 3 NMOS	0	0	23	NA	No
[12]	No	Yes	1 DXCCII 3 NMOS	0	0	23	3.33	No
[13]	Yes	Yes	1 CCII 1 Op-amp	3	2	18 + 23	NA	No
[14]	Yes	Yes	1 CCII 1 UVC	2	2	20 + 40	NA	No
[15]	No	Yes	2 CCII	3	3	40 + 40	NA	No
[16]	Yes	Yes	2 CCII	2	1	18 + 18	NA	No
[17]	No	Yes	2 CCII	2	1	2*21	NA	No
[18]	No	Yes	2 CCII 1 Buffer	4	1	18 + 8	NA	No
[19]	No	No	1 CCII−	2	1	16	NA	No
[20]	Yes	Yes	1 CCII 28 MOS	1	1	38	5.2	No
[21]	Yes	Yes	2 DVCC	2	2	2*12	0.93	No
[26]	No	Yes	1 Translinear loop 2 Current mirrors	2	2	8	NA	Yes
[27]	No	No	1 CCII+ 2 Current mirrors	2	2	17	NA	Yes
[28]—I	No	Yes	4 CCCII	5	3	4*15	NA	Yes
[28]—II	No	Yes	3 CCCII	5	2	3*15	NA	Yes
This work	Yes	Yes	2 CFOA 3 or 2 NMOS	0 or 1	0 or 1	2*18 + 3(or 2)	1.33	Yes

NA not available, *CCII* 2nd generation current conveyor, *DO-OTA* dual-output operational transconductance amplifier, *DXCCII* Dual-X 2nd generation current conveyor, *UVC* universal voltage conveyor, *DVCC* differential voltage current conveyor, *CCCII* current controlled 2nd generation current conveyor, *CFOA* current feedback operational current conveyor

Also, terminal X of the first CFOA can produce a current passing through the NMOS transistor M_A which can be given as follows:

$$I_{DA} = \frac{k_n}{2}\left(V_{Tn} - V_{in}(t)_{-} - V_{Tn}\right)^2 = \frac{k_n}{2}\left(V_{in}(t)_{-}\right)^2 \quad (6)$$

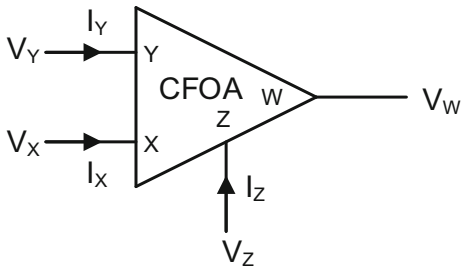

Fig. 2 Electrical symbol of the CFOA

According to the terminal relationship of the CFOA given in Eqs. (1), a current with the same direction can pass through M_C whose value is given in Eq. (3). Then,

$$I_{DC} = I_{DA} \tag{7}$$

As a result,

$$V_o(t) = -V_{in}(t)_- \tag{8}$$

One can express the input voltage of the proposed full-wave rectifier as

$$V_{in}(t) = V_{in}(t)_+ + V_{in}(t)_- \tag{9}$$

Here, $V_{in}(t)_-$ and $V_{in}(t)_+$ are negative and positive cycle of the input signal, respectively, given as

$$V_{in}(t)_- = \begin{cases} -V_{in}(t) & for\ V_{in}(t) \le 0 \\ 0 & otherwise \end{cases} \tag{10a}$$

$$V_{in}(t)_+ = \begin{cases} V_{in}(t) & for\ V_{in}(t) \ge 0 \\ 0 & otherwise \end{cases} \tag{10b}$$

From Eqs. (5) and (8), output voltage of the proposed full-wave rectifier can be given as

$$V_o(t) = |V_{in}| \tag{11}$$

Thus, the proposed circuit demonstrated in Fig. 3 can be considered as a full-wave rectifier circuit. If the NMOS transistor, M_C in the rectifier circuit of Fig. 3 is replaced by a resistor, R as shown in Fig. 4 and according to the Eqs. (2) and (4), the output voltage for the positive cycle of the input signal across the resistor, R can be expressed by:

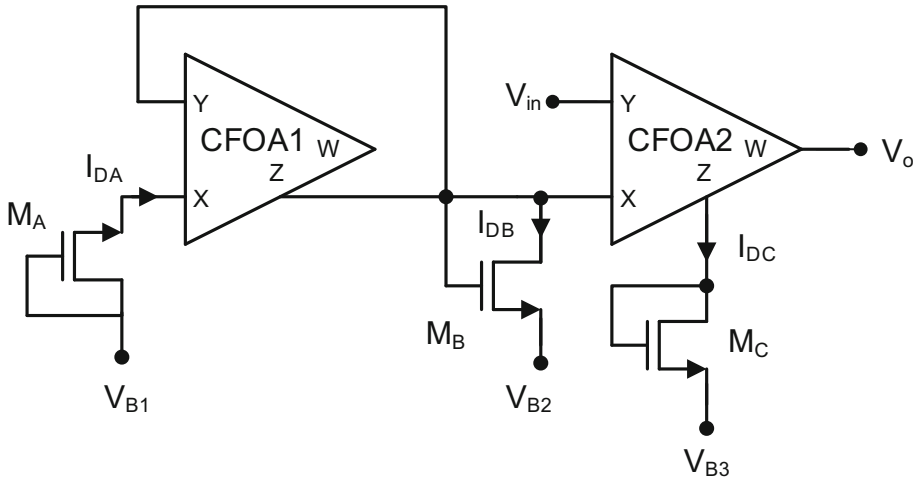

Fig. 3 The proposed full-wave rectifier structure

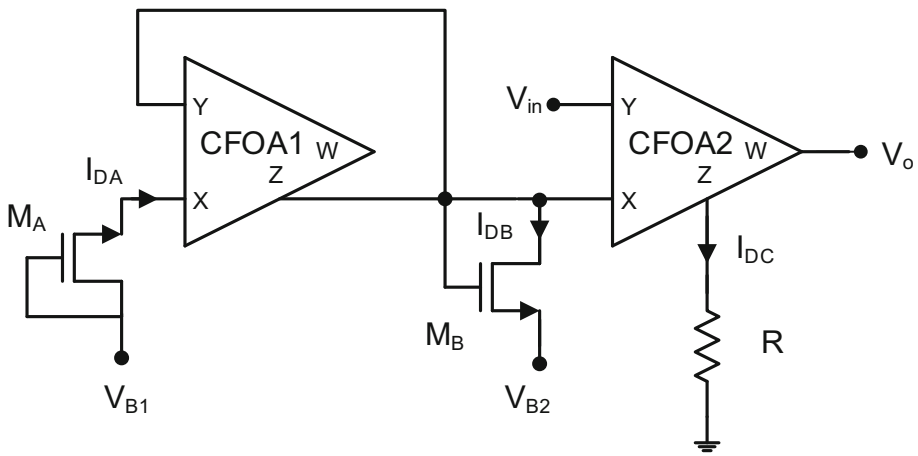

Fig. 4 The proposed sinusoidal frequency doubler circuit

$$V_o(t) = \frac{Rk_n}{2}\left(V_{in}(t)_+\right)^2 \tag{12}$$

Similarly, output voltage for the negative cycle of the input signal across the resistor, R can be expressed as:

$$V_o(t) = \frac{Rk_n}{2}\left(V_{in}(t)_-\right)^2 \tag{13}$$

According to Eq. (9), the following output voltage for the proposed sinusoidal frequency doubler can be obtained:

$$V_o(t) = \frac{Rk_n}{2}\left(|V_{in}(t)|\right)^2 \tag{14}$$

In other words, the proposed circuit given in Fig. 4 can be considered as a voltage signal squarer circuit. For a sinusoidal input signal voltage $V_{in}(t) = V_m \sin \omega t$, Eq. (14) can be re-written as

$$V_o(t) = \frac{Rk_nV_m^2}{2}(\sin \omega t)^2 = \frac{Rk_nV_m^2}{4}(1 - \cos 2\omega t) \tag{15}$$

It is clearly seen from Eq. (15) that the frequency of the output voltage $V_o(t)$ of the circuit of Fig. 4 is twice the input signal frequency, without any harmonic components unlike those presented in the voltage equations of the circuits in [8, 26, 27]. Equation (15) can be re-arranged and written as in the following:

$$V_o(t) = V_{DC} - V_{2m}\cos 2\omega t \tag{16}$$

where $V_{DC} = \frac{Rk_nV_m^2}{4}$ is a DC component and $V_{2m} = \frac{Rk_nV_m^2}{4}$ is the peak value of the AC component. The above equation indicates that the output voltage contains a DC component and a signal voltage with a frequency that is twice the frequency of the input signal. Thus, the proposed circuit given in Fig. 4 can be considered as a sinusoidal frequency doubler circuit.

It is worth noting that in the realization of the CFOA based rectifier, one should be careful about the input signal level. For a linear operation, according to Eqs. (2) and (6), the current of each NMOS transistor should not exceed the following limit in order to make operations of the CFOAs linearly [11]:

$$|\mathrm{V_{in}}| \le \sqrt{\frac{2\min\{\mathrm{I_{Xmax}}, \mathrm{I_{Zmax}}\}}{\mathrm{k_n}}} \tag{17}$$

where $\mathrm{I_{Xmax}}$ and $\mathrm{I_{Zmax}}$ are the maximum acceptable current for linear operation of the terminal X and the terminal Z of the CFOA, respectively.

3 Analysis of non-ideality effects of the CFOA

If the non-ideal gains stemmed from the physical realization of the CFOA are considered, the terminal characteristics in Eqs. (1) of the CFOA can be changed as

$$I_Y = 0 \tag{18a}$$

$$V_X = \beta V_Y \tag{18b}$$

$$I_Z = \alpha I_X \tag{18c}$$

$$V_W = \gamma V_Z \tag{18d}$$

where $\beta = 1 - \varepsilon_{vi}$, ε_{vi} represents the input voltage tracking error, $\alpha = 1 - \varepsilon_i$, ε_i represents the current tracking error and $\gamma = 1 - \varepsilon_{vo}$, ε_{vo} represents the output voltage tracking error. Here, $|\varepsilon_{vi}| \langle\langle 1$, $|\varepsilon_i| \langle\langle 1$ and $|\varepsilon_{vo}| \langle\langle 1$ and β, α, and γ are

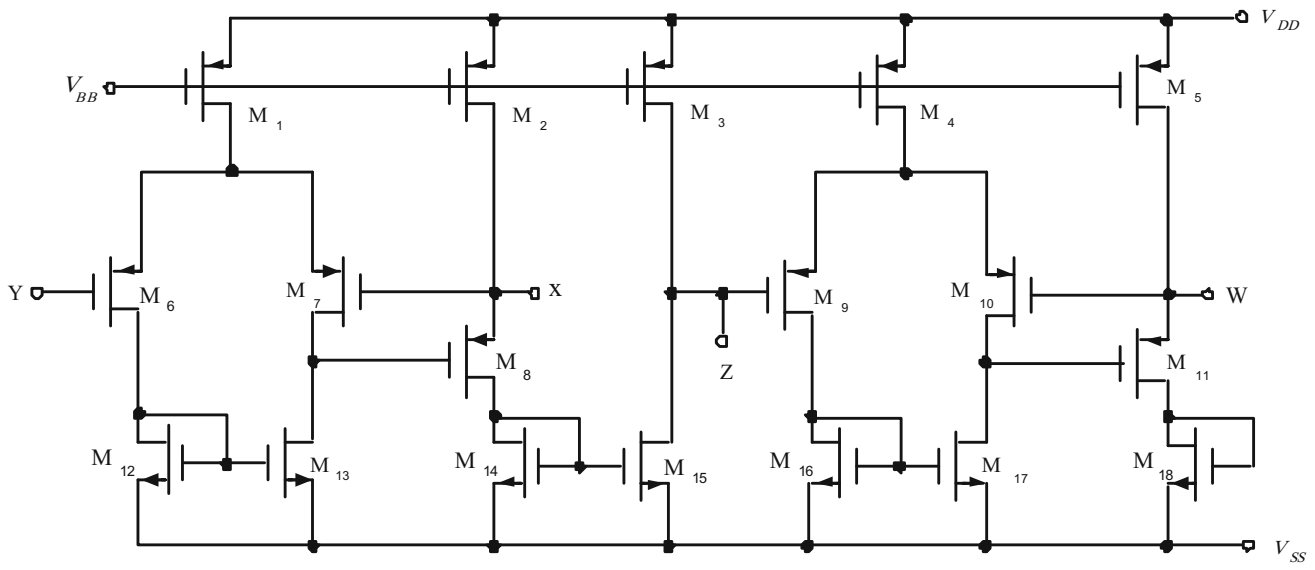

Fig. 5 MOS transistor based realization of the CFOA derived from one given in [29]

Table 2 MOS transistor aspect ratios of the CFOA circuit demonstrated in Fig. 4

Transistor name	W/L (μm)
M_1–M_7, M_9, M_{10}	40/0.5
M_8 and M_{11}	200/0.5
M_{12}–M_{18}	13/0.5

Table 3 Transistor aspect ratios of the NMOS transistors given in the rectifier and frequency doubler circuits respectively depicted in Figs. 2 and 3

Transistor name	W/L (μm)
M_A, M_B and M_C	40/0.5

frequency dependent quantities and ideally equal to unity. If non-ideal voltage and current gains are taken into account, Eqs. (2) through (5) can be given as in the following:

$$I_{DB} = \frac{k_n}{2}\left(\beta_2 V_{in}(t)_+ + V_{Tn} - V_{Tn}\right)^2 = \frac{k_n}{2}\left(\beta_2 V_{in}(t)_+\right)^2 \tag{19a}$$

$$I_{DC} = \frac{k_n}{2}\left(\frac{1}{\gamma_2}V_o(t) + V_{Tn} - V_{Tn}\right)^2 = \frac{k_n}{2}\left(\frac{1}{\gamma_2}V_o(t)\right)^2 \tag{19b}$$

$$I_{DC} = \alpha_2 I_{DB} \tag{19c}$$

Table 4 Some parameters of the CFOA given in Fig. 4

Parameter	Value
R_x	4 Ω
R_z	54 kΩ
R_y	∞
C_y	35 fF
C_z	89 fF
Bandwidth of V_X/V_Y	592 MHz
Bandwidth of I_Z/I_X	335 MHz
Bandwidth of V_w/V_z	574 MHz
Power supply voltages	±1.25 V
V_{BB}	0.4 V
Voltage gain (β)	0.989
Current gain (α)	1.024
Voltage gain (γ)	0.989

$$V_o(t) = \sqrt{\alpha_2}\beta_2\gamma_2 V_{in}(t)_+ \tag{19d}$$

Likewise, for the negative cycle of the input voltage the Eqs. (6) and (7) can be re-written as

$$I_{DA} = \frac{k_n}{2}\left(V_{Tn} - \beta_1\beta_2 V_{in}(t)_- - V_{Tn}\right)^2 = \frac{k_n}{2}\left(\beta_1\beta_2 V_{in}(t)_-\right)^2 \tag{20a}$$

$$I_{DC} = \alpha_1\alpha_2 I_{DA} \tag{20b}$$

$$V_o(t) = -\sqrt{\alpha_1\alpha_2}\beta_1\beta_2\gamma_2 V_{in}(t)_- \tag{20c}$$

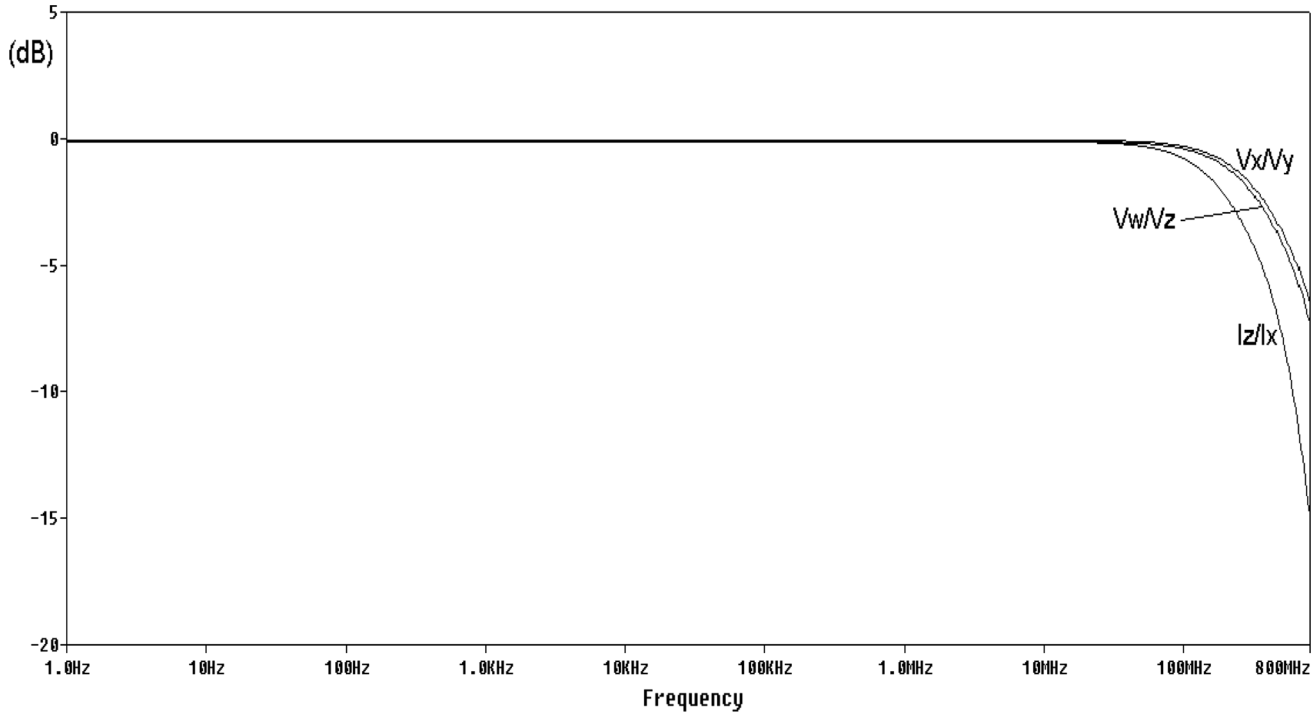

Fig. 6 Frequency response of the of the CFOA terminals

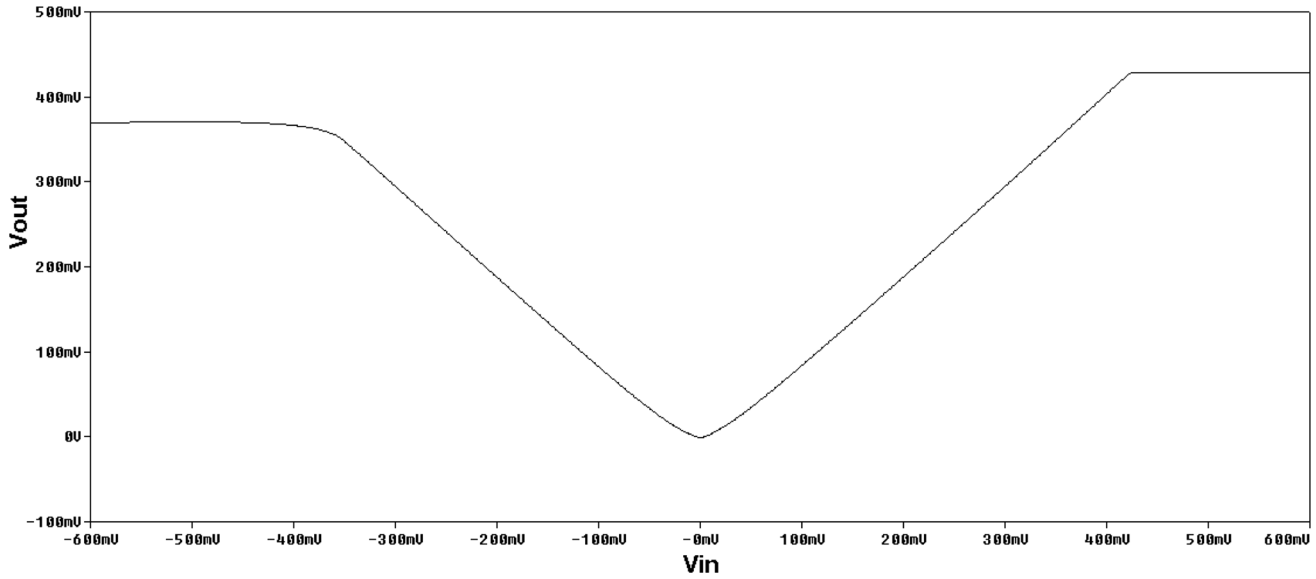

Fig. 7 DC transfer characteristic of the proposed full-wave rectifier structure

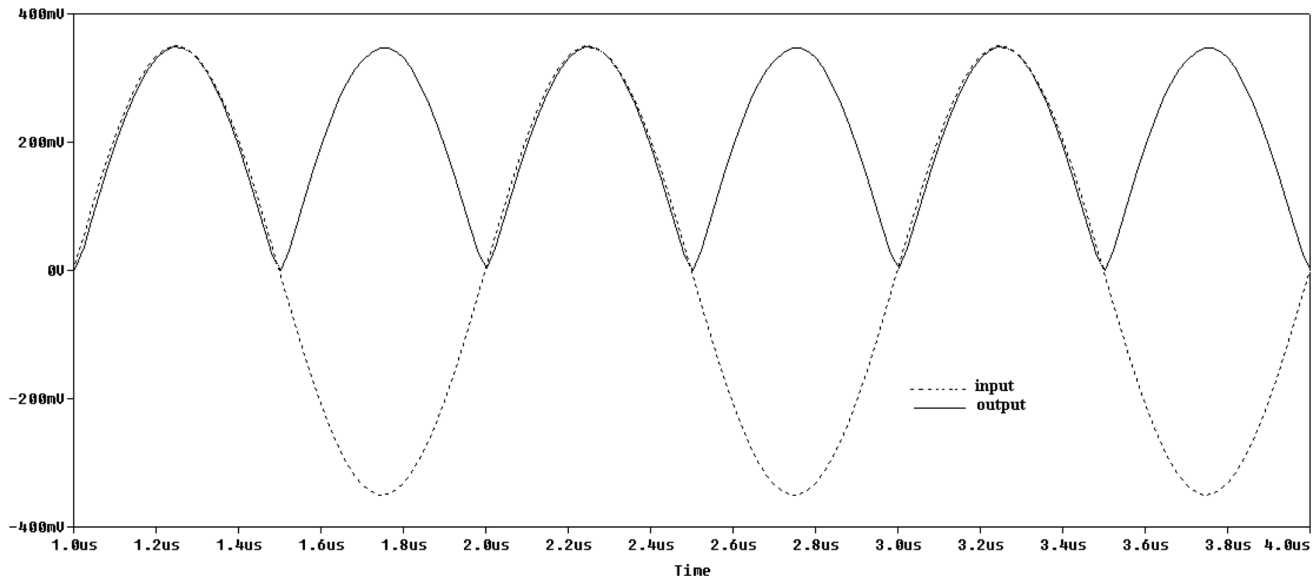

Fig. 8 Transient response of the full-wave rectifier structure at $f = 1$ MHz and $V_p = 350$ mV

Therefore, the complete equation of the output voltage can be given as

$$\begin{aligned} V_o(t) &= \sqrt{\alpha_2}\beta_2\gamma_2 V_{in}(t)_+ - \sqrt{\alpha_1\alpha_2}\beta_1\beta_2\gamma_2 V_{in}(t)_- \\ &= \sqrt{\alpha_2}\beta_2\gamma_2\left(V_{in}(t)_+ - \sqrt{\alpha_1}\beta_1 V_{in}(t)_-\right) \end{aligned} \tag{21}$$

From above equation, it can be observed that the gain of the both half cycles of the input voltage signal cannot be identical; therefore, special care should be taken in the implementation of the CFOA to ensure the output voltage given in Eq. (11). Note that the current tracking errors caused by α_1 and α_2 can be compensated by slightly adjusting the biasing voltages of the NMOS transistors, V_{B1} and V_{B2}, respectively, which determines the current of the drain of the NMOS transistors. Similarly, the effect of the non-ideal gains of the CFOA can be shown for the frequency doubler circuit as:

$$\begin{aligned} V_o(t) &= \frac{Rk_n\alpha_2\gamma_2}{2}\left(\beta_2 V_{in}(t)_+\right)^2 + \frac{Rk_n\alpha_1\alpha_2\gamma_2}{2}\left(\beta_1\beta_2 V_{in}(t)_-\right)^2 \\ &= \frac{Rk_n\alpha_2\gamma_2\beta_2^2}{2}\left(\left(V_{in}(t)_+\right)^2 + \alpha_1\beta_1^2\left(V_{in}(t)_-\right)^2\right) \end{aligned} \tag{22}$$

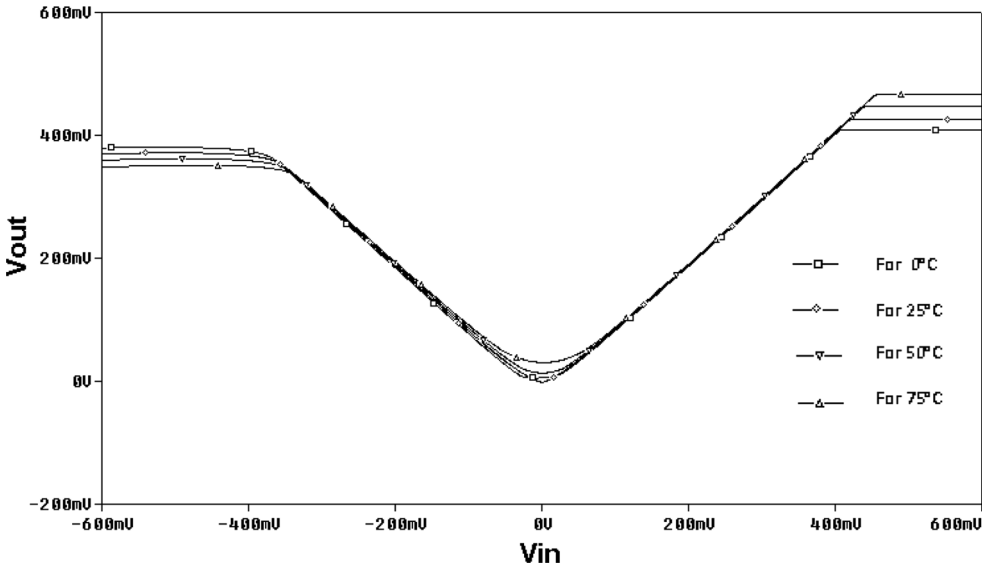

Fig. 9 DC temperature analysis of the proposed full-wave rectifier structure

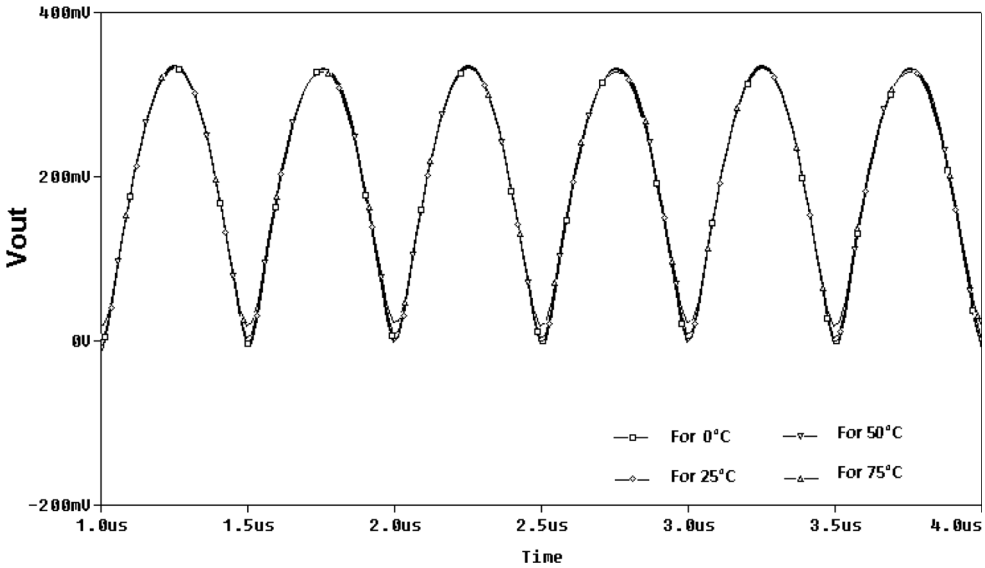

Fig. 10 Transient temperature analysis of the proposed full-wave rectifier structure

From above equation, it can be observed that the gain factor of squaring of the both half cycles of the input voltage signal cannot be identical. Consequently, for a sinusoidal input signal voltage $V_{in}(t) = V_m \sin \omega t$, Eq. (22) can be written as

$$V_o(t) = V_{DCn} - \left(V_{2mp} cos2\omega t_+ + V_{2mn} cos2\omega t_-\right) \tag{23}$$

where $V_{DCn} = \frac{Rk_n \alpha_2 \gamma_2 \beta_2^2 V_m^2}{4}$ is a DC component and $V_{2mp} = \frac{Rk_n \alpha_2 \gamma_2 \beta_2^2 V_m^2}{4}$ and $V_{2mn} = \frac{Rk_n \alpha_1 \alpha_2 \gamma_2 \beta_1^2 \beta_2^2 V_m^2}{4}$ are the peak values of the positive and the negative half cycles of the AC component, respectively. This means that, due to the non-ideal characteristic of the CFOA, the amplitude of the both half cycles of the output voltage $V_o(t)$ is slightly deviated from the ideal case of Eq. (16) by the factor $\alpha_2 \gamma_2 \beta_2^2$ for the DC component and positive half cycle of the AC component as well as $\alpha_1 \alpha_2 \gamma_2 \beta_1^2 \beta_2^2$ for the negative half cycle of the AC component.

4 Simulation results

SPICE simulation program is used in this work in order to verify the theoretical design. In order to accomplish simulations, the CFOAs are realized with the CMOS structure demonstrated in Fig. 5 that is adopted from the structure given in [29]. Further, DC symmetrical supply voltages and bias voltage are respectively chosen as ± 1.25 V and $V_{BB} = 0.4$ V. For the simulation purpose, 0.25 µm TSMC CMOS technology process parameters given in [21] are

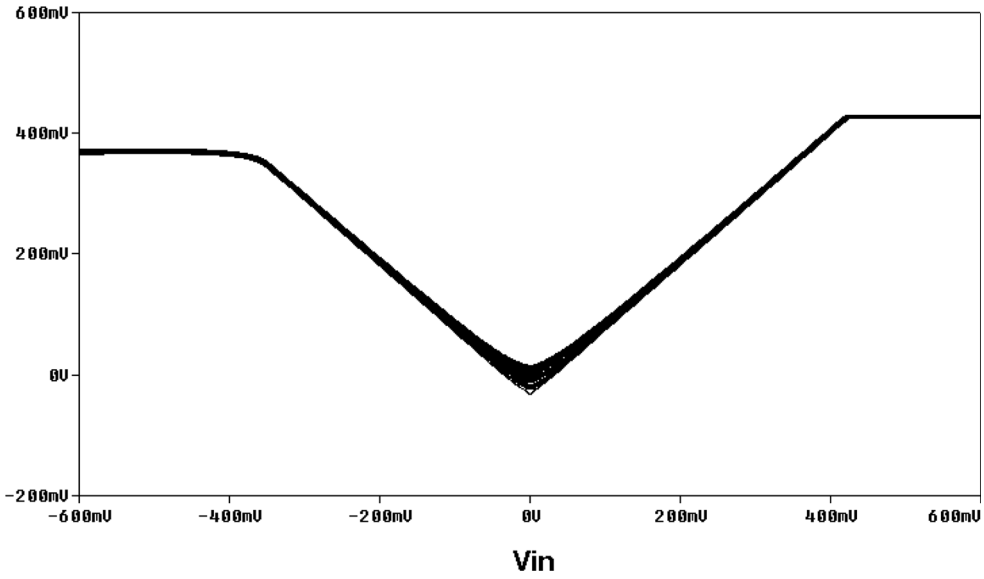

Fig. 11 DC Monte Carlo analysis of the proposed full-wave rectifier structure

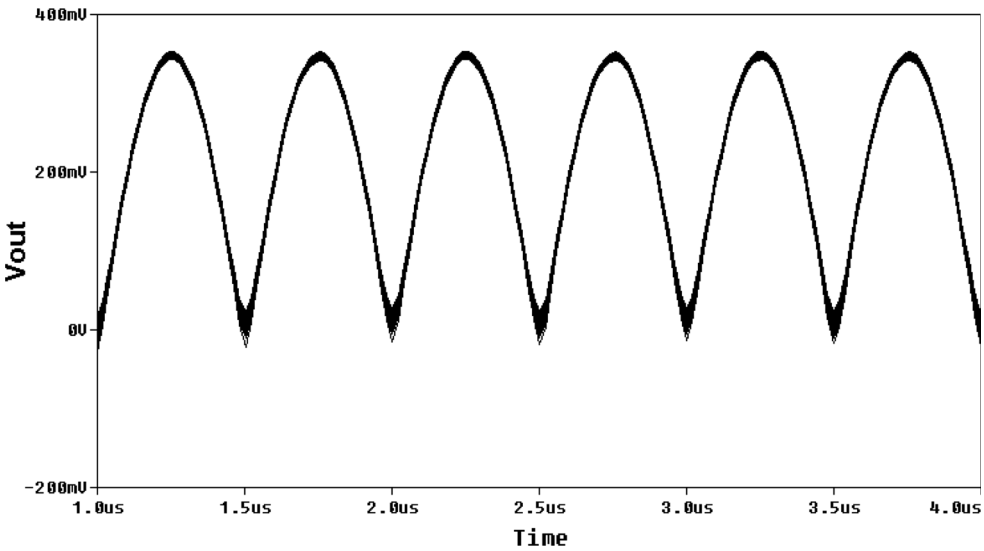

Fig. 12 Transient Monte Carlo analysis of the proposed full-wave rectifier structure

used. The dimensions of the MOS transistors used in the CFOA structure of Fig. 4 and the dimensions of the NMOS transistors used in the full-wave rectifier and frequency doubler circuits are given in Tables 2 and 3, respectively. $V_{B1} = -V_{B2} = 0.431$ V and $V_{B3} = -0.455$ V are chosen, which are slightly higher than V_{Tn} in order to compensate the current gain differences resulted from the non-ideality of the CFOAs as explained in Sect. 3.

The voltage gain frequency responses of the input voltage follower part, the current gain of the current follower part and the voltage buffer of the output part of the CFOA are illustrated in Fig. 6. The cutoff frequencies of the input voltage follower part (V_X/V_Y), the current follower part (I_Z/I_X) and the output voltage buffer (V_W/V_Z) of the active element are found as 593, 335 and 574 MHz, respectively. A summary of the CFOA element parameters used for the simulations are depicted in Table 4.

The DC voltage transfer function of the rectifier is shown in Fig. 7. It can be seen that that the maximum magnitude of the input voltage signal can be approximately 350 mV in magnitude. Outer this range of the input voltage, the transistors in the input stages of the CFOA implemented by the configuration given in Fig. 5 are no longer operated in the saturation region. The nonzero output voltage is approximately -750 μV, which is observed from Fig. 7. The nonzero output voltage is result of the mismatches in the differential pairs of the input stage of the CFOA structure in Fig. 5 and the error caused by unbalanced output resistances of the transistor M_2, M_8 and M_{14}. Transient response of the rectifier circuit given in

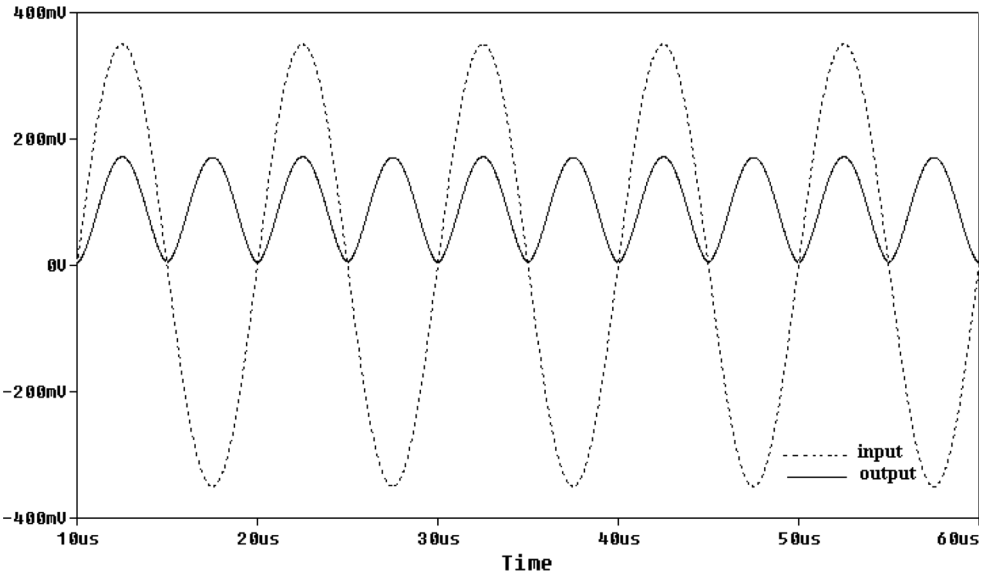

Fig. 13 Transient response of the proposed sinusoidal frequency doubler structure at f = 100 kHz and V_{p-p} = 0.7 V

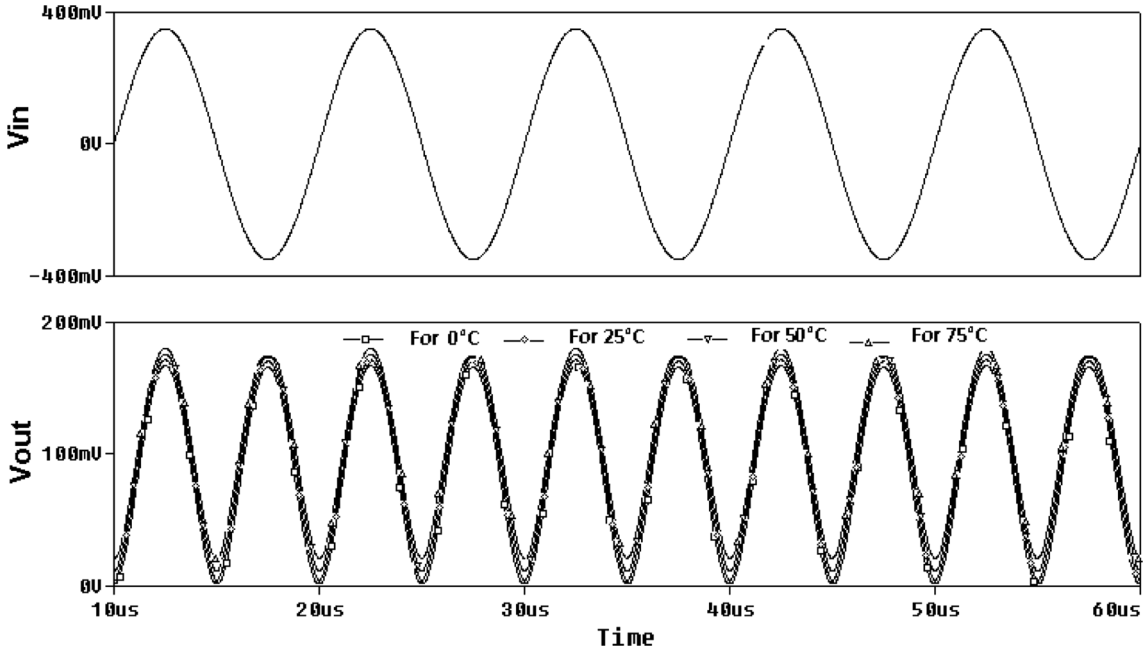

Fig. 14 Transient temperature analysis of the proposed sinusoidal frequency doubler structure

Fig. 3 for an input voltage signal with 350 mV peak and a frequency of $f = 1$ MHz is demonstrated in Fig. 8. DC and transient temperature analyses of the proposed rectifier circuit are shown in Figs. 9 and 10, respectively, where temperature is varied from 0 to 75 °C by a step size of 25 °C. Moreover, the DC and transient Monte Carlo (MC) analyses after 50 runs by changing 0.15% of the value of the threshold voltages of all of the MOS transistors are given in Figs. 11 and 12, respectively.

The performance of the proposed sinusoidal frequency doubler circuit given in Fig. 4 is shown in Fig. 13. The peak to peak amplitude of V_{in} is 0.7 V, the test frequency is 100 kHz, and resistance value of R is chosen as 1 kΩ. DC temperature analysis of the frequency doubler circuit is shown in Fig. 14 where temperature is varied from 0 to 75 °C by a step size of 25 °C. Further, the transient MC analysis after 50 runs by changing 0.15% of the value of the threshold voltages of all of the MOS transistors is given in Fig. 15.

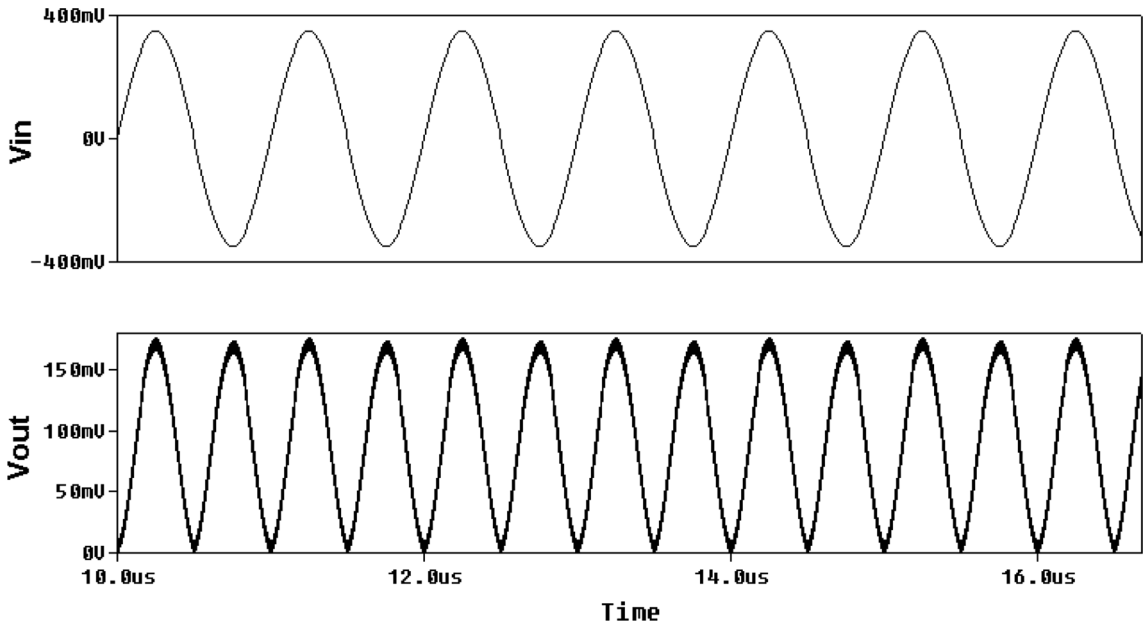

Fig. 15 Transient Monte Carlo analysis of the proposed sinusoidal frequency doubler structure

5 Conclusion

In this manuscript, a new VM full-wave rectifier and sinusoidal frequency doubler topology is proposed. It has the following properties: high input and low output impedances, employing only two CFOAs and only three NMOS transistors for the full-wave rectifier configuration and using only two CFOAs, two NMOS transistors and one grounded resistor for the sinusoidal frequency doubler circuit. Low output and high input impedance properties for both circuits are advantageous for easy cascading with other VM ones. No need to use any passive element in the rectifier circuit and usage only one resistor which is grounded are advantageous in integrated circuit realization point of view. Unlike previously reported sinusoidal frequency doubler circuits, the proposed one in this paper does not contain harmonics in its output voltage signal which decreases the non-linearity noise at the output signal. The SPICE simulation results verify the expected operation of the proposed circuits. Nevertheless, the slight difference between ideal and simulation results mainly stems from non-ideal gains of the CFOAs. DC temperature and MC analyses show the acceptability of the circuit responses for possible temperature and threshold voltage changes.

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