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DVCC-based floating capacitance multiplier design

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Abstract: In this paper, a floating capacitance multiplier including two multioutput differential voltage current conveyors, two grounded resistors, and a grounded capacitor is proposed. The proposed floating capacitance multiplier can realize high capacitor values with two small-valued resistors. It is more suitable for integrated circuit technology because it has only grounded passive components without needing any critical passive component matching conditions. Its performances are examined with several simulations using the SPICE program. As an application example, a third-order notch filter using three resistors and three capacitors is given.

Key words: Floating capacitance multiplier, differential voltage current conveyor, notch filter

1. Introduction

Large-valued capacitors that have good linearity and accuracy are used in many analog integrated circuits such as fully integrated phase-locked loops, sample-and-hold data systems, and radio frequency building blocks [1,2]. Metal-to-poly and metal-to-metal capacitors possess good linearity. However, they suffer from bigger fractional die areas for many standard silicon-based technologies [3,4]. Thus, active device-based capacitance multiplier design is used to obtain large-valued capacitors for standard silicon-based technology. There are a number of capacitance multiplier circuits implemented with some active devices such as operational amplifiers [5,6], second-generation current conveyors (CCIIs) or current-controlled current conveyors (CCCIIs) [7–17], operational transconductance amplifiers (OTAs) [18–20], current follower transconductance amplifiers (CFTAs) [21], tunable four terminal floating nullors (TFTFNs) [22], current-controlled differential difference current conveyors (CCDDCCs) [23], differential voltage current conveyors (DVCCs) [24–29], fully differential voltage and current gained second-generation current conveyors (FD VCG-CCIIs) [30], differential voltage current conveyor transconductance amplifiers (DVCCTA) [31], voltage differencing current conveyors (VDCCs) [32], and current controlled current conveyor transconductance amplifier (CCCCTAs) [33]. Some previously published capacitance multipliers [5,10,13,17,24] need large-valued resistors for large-valued capacitors. The other capacitance multipliers [9,12,16,18–23,27,28] require large currents to obtain large capacitor values. However, the proposed floating capacitance multiplier can realize large capacitor values with two small-valued resistors. The dynamic range of OTAs using bias currents is limited and therefore OTA-based capacitance multipliers have dynamic range problems [9]. The CCIIs and DVCCs [34], which have larger linearity and dynamic range, are attractive devices for obtaining capacitance multipliers. However, the conventional CCIIs are not convenient active blocks for building differential inputs. DVCCs have differential signal operation capability due to differential

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inputs. Capacitance multiplier designs with DVCCs are also easy and versatile [26]. A floating capacitance multiplier designed with two MODVCCs, two grounded resistors, and a grounded capacitor is proposed in this study. The proposed floating capacitance multiplier can be constructed with one MODVCC, one plus-type CCCII (CCCII+) [35], one tunable resistor [36–38], and a grounded capacitor, while the multipliers given in [5,10,12,13,17,24,28,32] are designed with three or more passive components. The proposed floating capacitance multiplier does not require any critical passive component matching conditions. Some simulations with the SPICE program are performed to show the performance of the proposed capacitance multiplier.

2. The proposed floating capacitance multiplier

A DVCC can be easily realized by grounding the Y_3 terminal of the differential difference current conveyor (DDCC) [39], which has the properties of both a differential difference amplifier (DDA) and a CCII. The nonideal representation block of a multiple-output DVCC (MODVCC) and its internal structure are given in Figures 1 and 2, respectively. In nonideal conditions, a MODVCC can be defined by the following matrix equation:

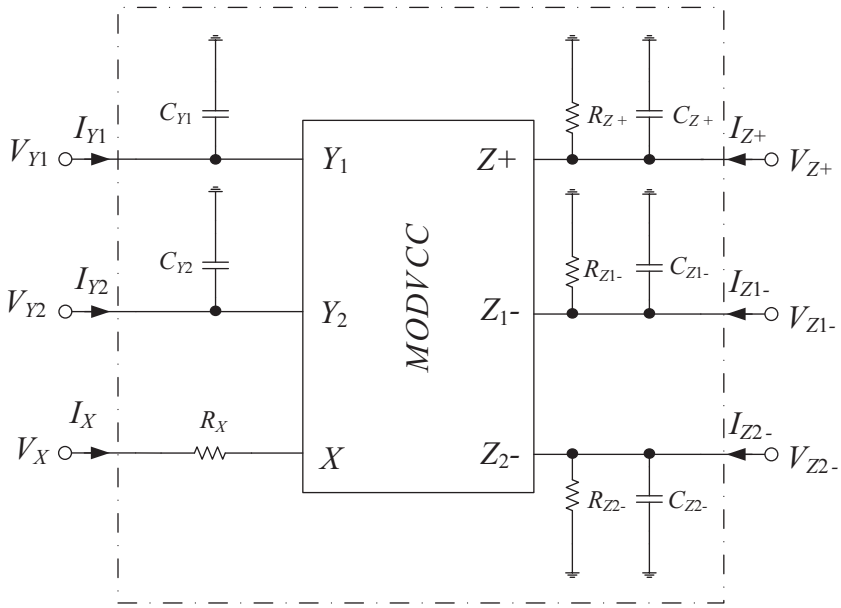

Figure 1. Nonideal MODVCC.

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z+} \\ I_{Z1-} \\ I_{Z2-} \end{bmatrix} = \begin{bmatrix} 0 & \beta & -\rho & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \alpha & 0 & 0 & 0 & 0 & 0 \\ -\gamma & 0 & 0 & 0 & 0 & 0 \\ -\eta & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z+} \\ V_{Z1-} \\ V_{Z2-} \end{bmatrix} \tag{1}$$

By using a single pole model [40], frequency-dependent nonideal current gains α, γ, and η and nonideal voltage gains β and ρ given in Eq. (1) can be defined as follows:

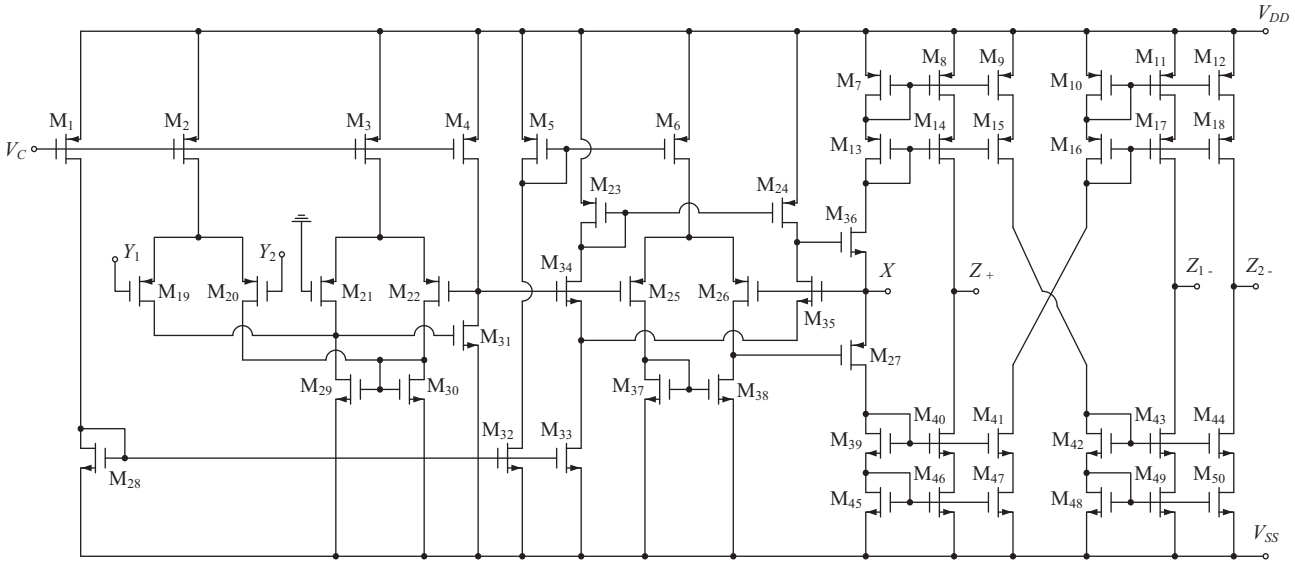

Figure 2. Internal structure of the MODVCC obtained from the ones in [34] and [39].

$$\alpha(s) = \frac{\alpha_0}{1 + s/\omega_\alpha}, \quad \gamma(s) = \frac{\gamma_0}{1 + s/\omega_\gamma}, \quad \eta(s) = \frac{\eta_0}{1 + s/\omega_\eta} \tag{2a}$$

$$\beta(s) = \frac{\beta_0}{1 + s/\omega_\beta}, \quad \rho(s) = \frac{\rho_0}{1 + s/\omega_\rho} \tag{2b}$$

DC nonideal current gains are described as $\alpha_0 = 1 + \varepsilon_\alpha$, $\gamma_0 = 1 + \varepsilon_\gamma$, $\eta_0 = 1 + \varepsilon_\eta$ where current tracking errors are defined as $|\varepsilon_\alpha| << 1$, $|\varepsilon_\gamma| << 1$ and $|\varepsilon_\eta| << 1$. Similarly, DC nonideal voltage gains are described as $\beta_0 = 1 + \varepsilon_\beta$, $\rho_0 = 1 + \varepsilon_\rho$ where voltage tracking errors are defined as $|\varepsilon_\beta| << 1$ and $|\varepsilon_\rho| << 1$. In ideal conditions, the DC nonideal gains are equal to unity while their bandwidths ω_α, ω_γ, ω_η, ω_β, and ω_ρ are ideally equal to infinity.

The internal structure given in Figure 2 is obtained from the ones in [34] and [41]. The proposed floating capacitance multiplier is shown in Figure 3. The input terminals of the circuit in [24] are taken from the X and Z/Y terminals while input terminals of the proposed one are taken from only the Z/Y terminals.

If only the X terminal parasitic resistor R_{Xi} (i= 1, 2) of the ith DVCCs is taken, the matrix equation is obtained as follows:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{sC}{(sCR_{X1} + 1) - \frac{R_1}{R_2 + R_{X2}}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{3}$$

Similarly, if only Z and Y terminal parasitic impedances of the DVCCs are taken, the matrix equation is obtained as below:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{R_2(1 + s(C + C_{Z2+})R_{Z2+})(R_{Z12-} + R_1(1 + s(C_{Y21} + C_{Z12-})R_{Z12-}))}{R_{Z2+}(R_2R_{Z12-} + R_1(R_2 + (s(C_{Y21} + C_{Z12-})R_2 - 1)R_{Z12-}))} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{4}$$

In Eq. (4), C_{Zi+} (i = 1, 2) and R_{Zi+} are the parasitic capacitor and parasitic resistor of the Z+ terminal of the ith DVCCs, respectively. R_{Zij-} (j = 1, 2) and C_{Zij-} are the parasitic resistor and parasitic capacitor of

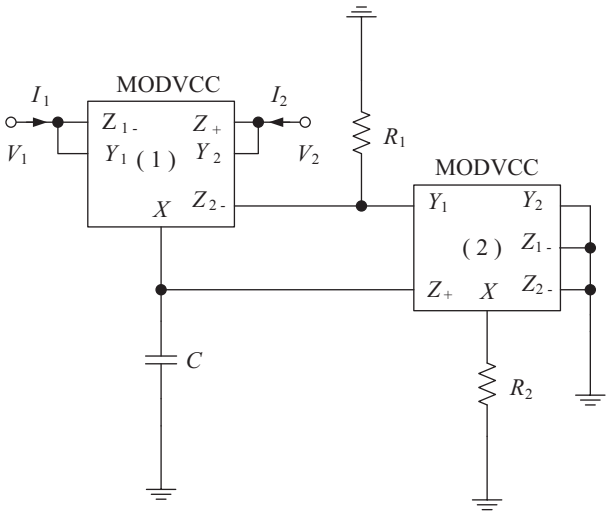

Figure 3. The proposed floating capacitance multiplier circuit.

the jth Z- terminal of the ith DVCC. Furthermore, C_{Yij} is the parasitic capacitor of the jth Y terminal of the ith DVCC. If only nonideal gains are taken into account, the matrix equation is obtained as follows:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{sC}{1-\frac{R_1\alpha_2\beta_2\eta_1}{R_2}} \begin{bmatrix} \beta_1\gamma_1 & -\rho_1\gamma_1 \\ -\beta_1\alpha_1 & \rho_1\alpha_1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{5}$$

Here, the equivalent capacitor (C_{eq}) can be calculated as $C/(1-R_1/R_2)$ in ideal conditions. It is seen from the matrix equation in Eq. (5) that there are not any extra undesired series or parallel impedances due to nonideal gains. The operation frequency of the proposed capacitance multiplier given in Figure 2 can be calculated as $f \leq (0.1/2\pi)$ min $\{\omega_{\alpha1}, \omega_{\alpha2}, \omega_{\beta1}, \omega_{\beta2}, \omega_{\eta1}, \omega_{\gamma1}, \omega_{\rho1}\}$ [40]. From Eqs. (3) and (4), the frequency limitations [24] can be written as $f \leq 0.1 / (2\pi CR_{X1})$, $f \leq 0.1 / (2\pi(C+C_{Z2+})R_{Z2+})$, $f \leq 0.1 / (2\pi(C_{Y21}+C_{Z12-})R_{Z12-})$, and $f \leq 0.1 / (2\pi(C_{Y21}+C_{Z12-})R_2)$. It is observed from the above that the proposed capacitance multiplier has restrictions at high frequencies. The proposed capacitance multiplier and some other capacitance multiplier circuits are compared in Table 1.

3. Third-order filter application of the proposed capacitance multiplier

A twin-T notch filter [42] can be used as a feedback element in amplifiers, oscillators, and some other general purposes. The passive twin-T notch filter given in Figure 4 is chosen as an application for the proposed floating capacitance multiplier.

The transfer function (TF) for the twin-T notch filter given in Figure 4 can be obtained as follows:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a_3s^3+a_2s^2+a_1s+a_0}{b_3s^3+b_2s^2+b_1s+b_0} \tag{6}$$

Coefficients a_3, a_2, a_1, a_0, b_3, b_2, b_1, and b_0 of TF in Eq. (6) are calculated as follows:

Table 1. Previously published capacitance multipliers and the proposed one.

References	Technology	Used capacitor	Supply voltage	Used active device	Active device number	Passive component number	Matching condition	Power consumption of capacitance multiplier
[5]	NA	Grounded	NA	Op-Amp	2	5	No	NA
[9]	NA	Grounded	±2.5 V	CCCII+	4	1	No	NA
[10]	NA	Grounded	NA	CCII	4	3	No	NA
[12]	BJT	Grounded	±2.5 V	CCCII	≥ 3	4	No	NA
[13]	BJT	Grounded	±2.5 V	DO-CCII	2	3	No	NA
[16]	BJT	Grounded	±2.5 V	CCCII	4	1	No	NA
[17]	MOS/0.35 μm	Grounded	±1.5 V	CCII	3	4	Yes	NA
[18]	BJT	Grounded	±2.5 V	OTA	4	1	No	565 μW
[20]	MOS/Bi-MOS	Floating	NA	Op-Amp, OTA	5	1	No	NA
[21]	BJT	Grounded	±1.5 V	CFTA	4	1	No	NA
[22]	BJT	Floating	±10 V	TFTFN	2	1	No	NA
[23]	MOS/0.25 μm	Grounded	±1.25 V	CCDDCC	3	1	No	1.35 mW
[24]	MOS/0.35 μm	Grounded	±1.5 V	DVCC	2	3	No	NA
[27]	BJT	Grounded	±2.5 V	CCCII, DVCC	3	1	No	7.32 mW
[28]	BJT	Grounded	±1.5 V	CCCII, DVCC	4	3	No	NA
[30]	MOS/0.35 μm	Floating	±2 V	CCCCTA	1	1	No	≤ 3 mW
[31]	MOS/0.5 μm	Grounded	±2 V	DVCCTA	1	2	No	3 mW
[32]	MOS/90 nm	Grounded	±0.45 V	VDCC	2	3	No	NA
Proposed Circuit	MOS/0.13 μm	Grounded	±0.75 V	DVCC	2	3	No	1.29 mW

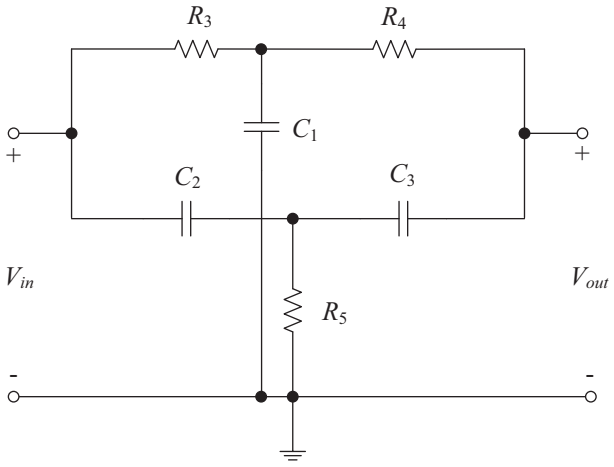

Figure 4. Passive RC twin-T notch filter.

$$
\begin{aligned}
&a_3 = b_3 = 1, \quad a_2 = \tfrac{1}{C_1}\left(\tfrac{1}{R_3} + \tfrac{1}{R_4}\right) \\
&a_1 = \tfrac{1}{C_1 R_3 R_4}\left(\tfrac{1}{C_2} + \tfrac{1}{C_3}\right), \quad a_0 = b_0 = \tfrac{1}{C_1 C_2 C_3 R_3 R_4 R_5} \\
&b_2 = \tfrac{1}{C_1}\left(\tfrac{1}{R_3} + \tfrac{1}{R_4}\right) + \tfrac{1}{C_2}\left(\tfrac{1}{R_4} + \tfrac{1}{R_5}\right) + \tfrac{1}{C_3 R_4} \\
&b_1 = \tfrac{1}{C_1 C_2}\left(\tfrac{1}{R_3 R_5} + \tfrac{1}{R_4 R_5} + \tfrac{1}{R_3 R_4}\right) + \tfrac{1}{C_3 R_4}\left(\tfrac{1}{C_1 R_3} + \tfrac{1}{C_2 R_5}\right)
\end{aligned} \tag{7}
$$

If the passive components are chosen as $C_1 = 2C$, $C_2 = C_3 = C$, $R_3 = R_4 = R$, and $R_5 = R/2$, the TF and the center rejection frequency (f_0) of the twin-T notch filter are respectively obtained as:

$$
\frac{V_{out}(s)}{V_{in}(s)} = \frac{s^3 + s^2\frac{1}{CR} + s\frac{1}{(CR)^2} + \frac{1}{(CR)^3}}{s^3 + s^2\frac{5}{CR} + s\frac{5}{(CR)^2} + \frac{1}{(CR)^3}} \tag{8}
$$

$$
f_0 = \frac{1}{2\pi RC} \tag{9}
$$

The proposed capacitance multiplier can be constructed by commercially available active devices as declared in [43].

4. Simulation results and discussions

In order to examine the performances of the proposed capacitance multiplier, some simulations by the SPICE program are achieved where 0.13 μm IBM CMOS technology parameters are used. Transistor sizes of the internal structure in Figure 2 are given in Table 2. The symmetrical DC power supply voltages and the bias voltage are chosen as ± 0.75 V and 0.37 V, respectively. In simulations, parasitic resistor and capacitor values of the DVCC are found as $R_X = 190\ \Omega$, $C_{Y1} = C_{Y2} = 15.9$ fF, $R_{Z+} = 1.69$ MΩ, $C_{Z+} = 31.8$ fF, $R_{Z1-} = R_{Z2-} = 1.68$ MΩ, and $C_{Z1-} = C_{Z2-} = 25.9$ fF.

Table 2. Transistor sizes for the internal structure given in Figure 2.

PMOS transistors	W (μm)	L (μm)
M_1	3.38	0.39
M_2, M_3, M_5, M_6 M_{19}, M_{20}, M_{25}, M_{26}	78	0.39
M_4, M_7–M_{18}, M_{21}–M_{24}, M_{27}	39	0.39
NMOS transistors	W (μm)	L (μm)
M_{28}–M_{32}, M_{36}–M_{50}	5.07	0.39
M_{33}–M_{35}	10.14	0.39

For the proposed floating capacitance multiplier given in Figure 3, simulations are performed by grounding the second terminal. The selected passive component values and the evaluated capacitance values are given in Table 3.

The capacitance value change with small-valued resistors of the proposed capacitance multiplier is shown in Figure 5. It is seen from Figure 5 that the operating frequency range of the proposed capacitance multiplier decreases for large multiplication factors. The proposed capacitance multiplier can increase the capacitance value up to 40 times. An electronically tunable grounded resistor [38] and a CCCII+ [44] are replaced instead

Table 3. Selected passive component values and corresponding capacitance values.

C	R_1	R_2	Capacitance values
50 pF	0.5 kΩ	1 kΩ	100 pF
	1.2 kΩ	1.6 kΩ	200 pF
	1.4 kΩ	1.6 kΩ	400 pF
	1.5 kΩ	1.6 kΩ	800 pF
	1.9 kΩ	2 kΩ	1 nF
	2.3 kΩ	2.4 kΩ	1.2 nF
	3.9 kΩ	4 kΩ	2 nF

of R_1 and the second MODVCC, respectively. Also, R_1 and R_2 are removed. Transistor sizes for the CMOS implementation of the CCCII+ [44] are given in Table 4. Transistor sizes for the electronically tunable grounded resistor are chosen as follows: $(W/L)_1 = (W/L)_2 = 1.3\ \mu$m/1.3 μm. Simulation results for the constructed capacitance multiplier with one MODVCC, one CCCII, one tunable resistor, and a grounded capacitor are given in Figure 6. On the other hand, the symmetrical DC power supply voltages for the CCCII+ and tunable resistor are chosen as ± 0.75 V. Control currents of the CCCII+ are varied between 0.8 μA and 12 μA.

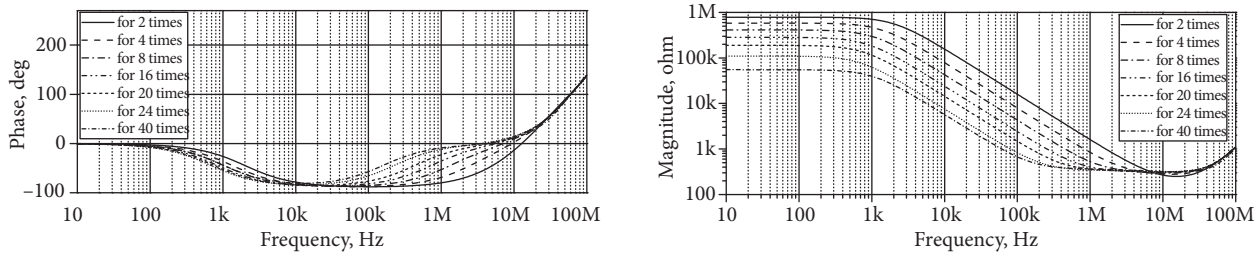

Figure 5. Phases and magnitudes of the impedances of the proposed capacitance multiplier established with MODVCC.

Table 4. Transistor sizes for internal structure of the CCCII+ [44].

PMOS transistors	W (μm)	L (μm)
M_3, M_4	3.9	0.39
M_5, M_6, M_{11}, M_{12}	1.3	0.39
NMOS transistors	W (μm)	L (μm)
M_1, M_2	1.65	0.39
M_7–M_{10}, M_{13}	0.78	0.39

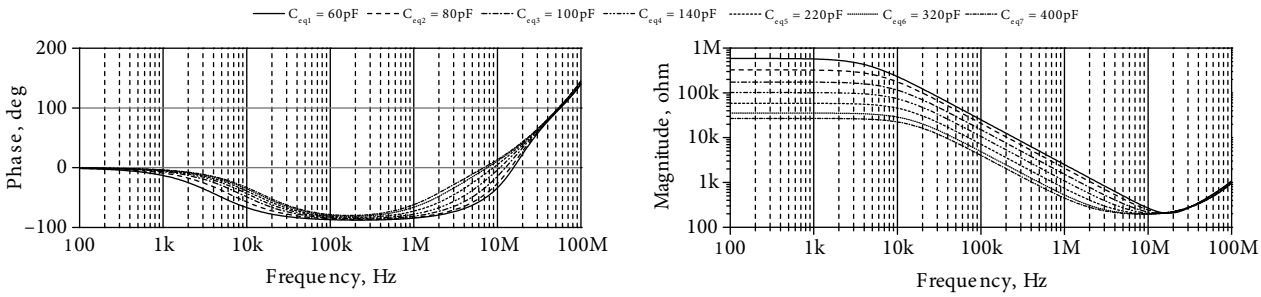

Figure 6. Phases and magnitudes of the impedances of the proposed capacitance multiplier established with MODVCC and CCCII [44].

In order to demonstrate the performance of the proposed floating capacitance multiplier, the proposed capacitance multiplier is replaced instead of each of the passive capacitors in the twin-T notch filter given in Figure 4. Passive component values for the passive and active twin-T notch filters are given in Table 5. The simulation results prove that the proposed capacitance multiplier shows good performance.

Table 5. The passive component values.

Passive twin-T notch		Active twin-T notch with the proposed capacitance multiplier		
R_3	8.2 kΩ	R_3	8.2 kΩ	Increment
R_4	8.2 kΩ	R_4	8.2 kΩ	
R_5	4.1 kΩ	R_5	4.1 kΩ	
C_1	1 nF	C_1 (R_1 = 1.8 kΩ and R_2 = 2 kΩ)	100 pF	10 times
C_2	500 pF	C_2 (R_1 = 1.4 kΩ and R_2 = 1.6 kΩ)	62.5 pF	8 times
C_3	500 pF	C_3 (R_1 = 1.2 kΩ and R_2 = 1.5 kΩ)	100 pF	5 times

The phase and gain simulation results for the twin-T notch filter given in Figure 4 are shown in Figure 7. The center rejection frequency is calculated as 38.8 kHz. The calculated value and obtained value from Figure 7 for f_0 are close to each other.

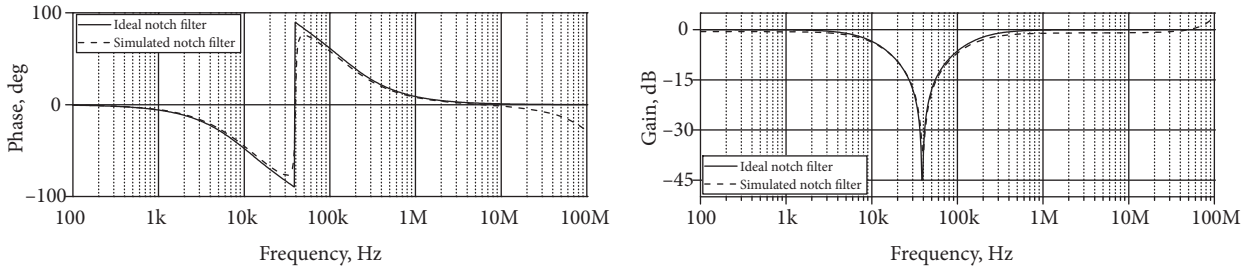

Figure 7. Phase and gain change of the filter in Figure 4 via frequency.

Circuit noise is undesirable for analog and digital systems. It is a cause of the deterioration of system accuracy [45]. Noise simulation results are given in Figure 8 for the twin-T notch filter.

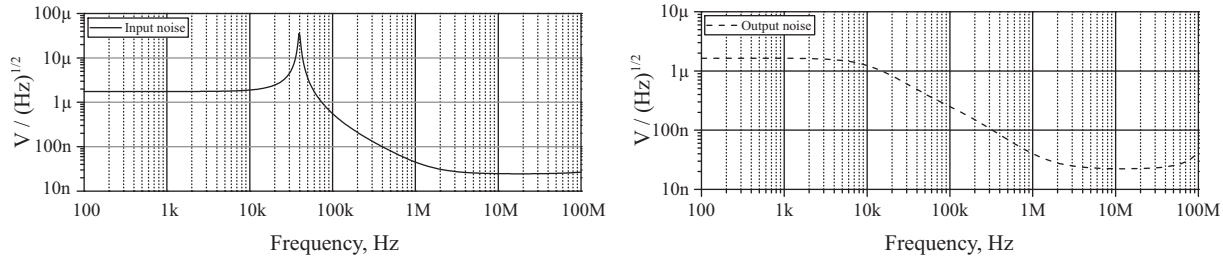

Figure 8. Input equivalent noise and the output noise change of the filter in Figure 4 via frequency.

A sinusoidal signal with 50 mV peak is applied to the twin-T notch filter at 8.8 kHz and 165 kHz frequencies separately. The obtained output signals corresponding to the input signal at 8.8 kHz and 165 kHz are given in Figure 9. Total harmonic distortion (THD) results are given in Figure 10.

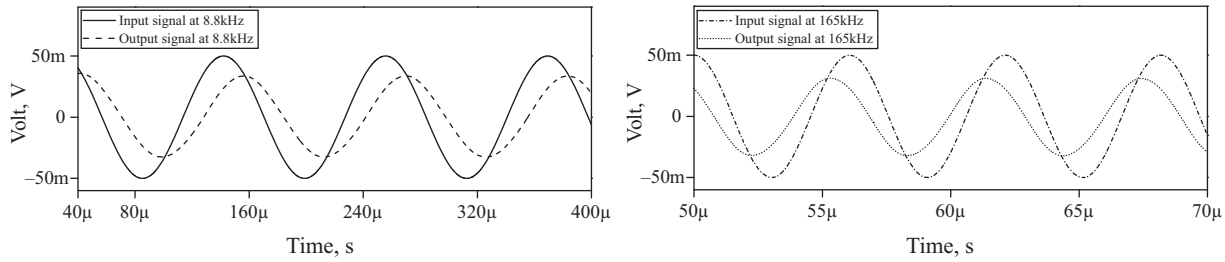

Figure 9. Output signals corresponding to input signals of the filter in Figure 4 at different frequencies.

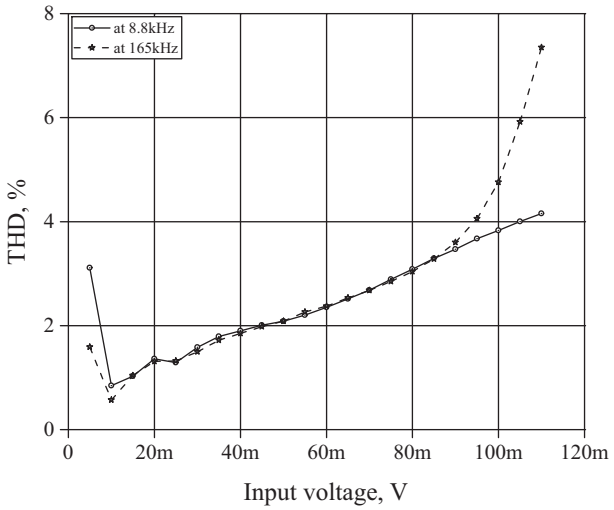

Figure 10. THD changes via sinusoidal peak input signals of the filter in Figure 4 at different frequencies.

THD for the twin-T notch filter is under 4% for the sinusoidal input signals between 5 mV and 92 mV peak at 165 kHz and for the sinusoidal input signals between 5 mV and 104 mV peak at 8.8 kHz. The total power dissipations are 1.29 mW and 3.91 mW for the proposed capacitance multiplier and the twin-T notch filter, respectively. The power dissipation of the twin-T notch filter application is a low value when compared to the filter applications given in [16,24,27,28]. The theoretical and simulation results are close to each other but the small difference between them can be attributed to nonidealities of the MODVCC.

5. Conclusion

A floating capacitance multiplier employing two MODVCCs, two grounded resistors, and a grounded capacitor is proposed. The proposed floating capacitance multiplier can realize large capacitor values with two small-valued resistors. It does not need any passive component matching conditions or cancellation constraints. Electronic controllability of the proposed floating capacitance multiplier can be achieved. The simulation results obtained with the SPICE program support the theory. The proposed floating capacitance multiplier configuration in this paper will be beneficial in a number of areas including communications and signal processing.

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