A novel DDCC+ based first-order current-mode active-C all-pass filter using a grounded capacitor

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Abstract: In this study, a novel first-order current-mode active-C all-pass filter based on a companding idea is proposed. In the design of the filter, a state space method is used. The proposed structure consists of only two plus-type differential difference current conveyors, nine external MOSFETs, and a single grounded capacitor. The dominant advantages of the proposed filter are briefly described as follows: offering resistorless design, consuming low power, having an electronic tunability property of its pole frequency, and not suffering from the disadvantage of any passive component matching conditions. By cascading two all-pass filters in a closed negative feedback loop, a high-Q band-pass network is designed as an application example. Several simulations including frequency domain and time domain analyses by using the PSpice program are carried out to confirm the theoretical design. All the obtained simulation results are given and discussed.

Key words: All-pass filter, current-mode, active-C, electronic tunability

1. Introduction

A differential difference current conveyor (DDCC) has the advantages of both a second-generation current conveyor and a differential difference amplifier [1]. The main specifications of the DDCC can be detailed as follows: higher accuracy, wide bandwidth, great dynamic range, and suitability for differential current-mode (CM) operations [1]. A number of first-order filter topologies based on DDCC providing various filter transfer functions (TFs) have been reported in the literature [2–7]. The previously published works used traditional voltage-mode (VM) synthesis methods [2–7] and CM synthesis methods [1]. Furthermore, the use of CM circuits offers a wider dynamic range when compared to that of VM circuits [8]. Recently, a DDCC based VM integrator circuit was presented in [9].

A DDCC is a nontunable active element [10] while some active devices such as second-generation current controlled current conveyors have the feature of electronic tunability with intrinsic resistors. A number of DDCC based filter structures are deprived of electronic tunability [2,4–6], but some DDCC based filter structures have the property of electronic tunability by adding extra circuitry [3,11,12]. In this paper, pole frequency of the proposed filter is controlled electronically by means of a DC control voltage source, without changing the bias condition of the active devices. Moreover, adaptive topologies enjoy externally controllable systems like the proposed filter.

CMOS integrated structures are mostly preferred in analog designs [13]. The types of passive components

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used in the integrated circuit topology design determine the category of architecture, such as active-R [14], active-C [11,15–21], active-RC [11], or active-only [22] circuits. Passive resistors, which have some disadvantages such as needing a large chip area and a nonaccurate current-voltage proportion, are not employed in the proposed circuit.

The companding design procedure enhances the dynamic range defined as the distance between lower and upper processable signal bounds. By keeping linearity, first the input signal is compressed, and afterwards the processing output signal is expanded. Therefore, the silicon area and power consumption are reduced considerably [23].

A novel active-C first-order all-pass (AP) filter structure using two plus-type DDCCs (DDCC+s), nine MOSFETs, and a grounded capacitor is proposed, which enjoys the following features: i) it uses two identical active devices, ii) it employs only a grounded capacitor as a passive component, iii) it does not need any passive component matching constraints, iv) its pole frequency can be controlled electronically, v) its signal processing algorithm is based on the companding method, vi) it possess advantages of CM circuits, and vii) it can be easily realized in IC technologies.

The paper is organized as follows: the design procedure of the proposed first-order AP filter is presented in Section 2. In this section, the architecture of the proposed circuit is described in detail. Section 3 deals with an application of the proposed AP filter. Some simulations and performance analyses of the proposed circuit are achieved in Section 4. In this section, PSpice simulations are performed in order to verify the theoretical results. Finally, some conclusions are given in Section 5.

2. The proposed circuit

The DDCC was first introduced in 1996 [1], and its arithmetic ability has been utilized by many researchers. The DDCC+ whose electrical symbol is shown in Figure 1 has five terminals. Using standard notation, the terminal relations of the DDCC+ can be characterized by the following hybrid matrix equation.

$$
\begin{bmatrix} v_X \\ i_{Y1} \\ i_{Y2} \\ i_{Y3} \\ i_Z \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{Y1} \\ v_{Y2} \\ v_{Y3} \\ i_X \end{bmatrix}
\tag{1}
$$

The TF of the proposed first-order AP filter is given in the following equation. In this equation, ω_o represents the angular pole frequency of the filter.

$$
H(s) = -\frac{s - \omega_o}{s + \omega_o}
\tag{2}
$$

In this paper, the state space synthesis method procedure provides very general solutions for realizing the AP filter whose TF is given in Eq. (2). In order to obtain the state space representation of the proposed first-order filter, it is transformed into the time domain. Converting Eq. (2) to the time domain, the following differential equation with constant coefficients is obtained.

$$
\dot{y} + \omega_o y = -\dot{u} + \omega_o u
\tag{3}
$$

Here, y and u indicate output and input signals, respectively. Dots above the variables denote the time differentiation. One way to get the state equation and output equation is to define the state space variable and
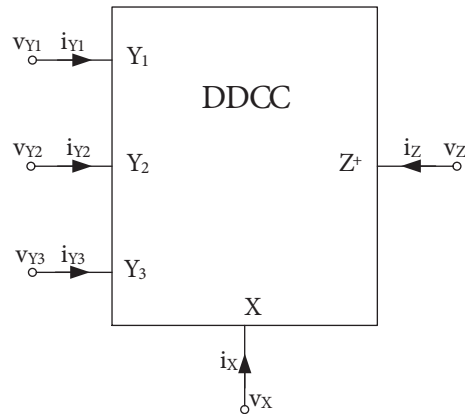
Figure 1. Electrical symbol of the DDCC+.

its derivative as given in Eq. (4) and Eq. (5), respectively.

$$x = y + ru \tag{4}$$

$$\dot{x} = \dot{y} + r\dot{u} \tag{5}$$

By substituting the last two equations into Eq. (3), a first-order differential equation that involves the derivative of the input signal can be obtained. In order to expose the general state space equation format of this linear first-order differential equation, the coefficient of the derivative of the input variable should be eliminated. By choosing $r = 1$, the state equation and output equation can be found as given in Eq. (6) and Eq. (7), respectively.

$$\dot{x} = -\omega_o x + 2\omega_o u \tag{6}$$

$$y = x - u \tag{7}$$

The next step of the filter synthesis, which is obtained by adopting the companding principle, is mapping the state space variable and input signal with a nonlinear function, $f(\bullet)$. The transformation function should provide certain requirements such as one-to-one and onto mapping.

$$x = f(v_x) \tag{8}$$

$$\dot{x} = \dot{f}(v_x) \tag{9}$$

$$u = f(v_u) \tag{10}$$

Substituting Eqs. (8)–(10) into Eqs. (6) and (7), Eq. (11) and Eq. (12) are yielded as follows.

$$\dot{f}(v_x) = -\omega_o f(v_x) + 2\omega_o f(v_u) \tag{11}$$

$$y = f(v_x) - f(v_u) \tag{12}$$

Multiplying both sides of Eq. (11) by $\frac{C}{f(v_x)}$, the following equation is obtained.

$$C\frac{\dot{f}(v_x)}{f(v_x)} = -\omega_o C + 2\omega_o C\frac{f(v_u)}{f(v_x)} \tag{13}$$

If the mapping function $f(\bullet)$ is chosen as exponential, the state equation and output equation respectively turn into Eq. (14) and Eq. (15), which are called circuit equations. In these equations, each term is considered as current in accordance with CM synthesis, which is the objective of this paper.

$$C\dot{v}_x = -I_{f1} + f(v_u + V_{f2} - v_x) \tag{14}$$

$$y = f(v_x) - u \tag{15}$$

Here, I_{f1} is a constant and the voltage of V_{f2} is defined as the inverse mapping function of I_{f2}, which is also a constant, $V_{f2} = f^{-1}(I_{f2})$.

These equations are the key aspect of the companding design procedure, briefly explained as three steps: compressing the input signal, processing the compressed signal, and expanding the processed signal, while keeping the linear relationship between the input signal and output signal.

In order to realize the proposed CM AP filter, the state variable and input signal are mapped to a more realistic function, which is the subthreshold current-voltage characteristic of the MOSFETs as given in Eq. (16) and Eq. (17). It can also be said that the function is only valid when the MOSFETs are operated in the "weak inversion region" [13].

$$x = f(v_x) = I_o e^{\frac{v_x}{\zeta V_T}} \tag{16}$$

$$u = f(v_u) = I_o e^{\frac{v_u}{\zeta V_T}} \tag{17}$$

Here, ζ is a nonideality factor that ranges from 1 to 3 and V_T is thermal voltage, defined as $V_T = kT/q$ [13]. The symbol k represents the Boltzmann constant, q is unit charge, and T is temperature.

Substituting the mapped state variable and input signal into Eq. (14) and Eq. (15), and after routine mathematical operations, circuit equations can be derived as given by Eq. (18) and Eq. (19).

$$C\dot{v}_x = -I_{f1} + I_o e^{\frac{v_u + V_{f2} - v_x}{\zeta V_T}} \tag{18}$$

$$y = I_o e^{\frac{v_x}{\zeta V_T}} - u \tag{19}$$

The proposed CM first-order AP filter consisting of two DDCC+s, nine external MOSFETs, and one grounded capacitor is given in Figure 2. As presented in the figure, the pole frequency of the first-order filter can be controlled by an external control voltage without needing any physical changes or requiring any passive component matching conditions. It should be emphasized that the proposed circuit can be classified in active-C topology (MOS-C) because of its resistorless architecture, which offers many advantages such as less chip area and low power consumption [18].
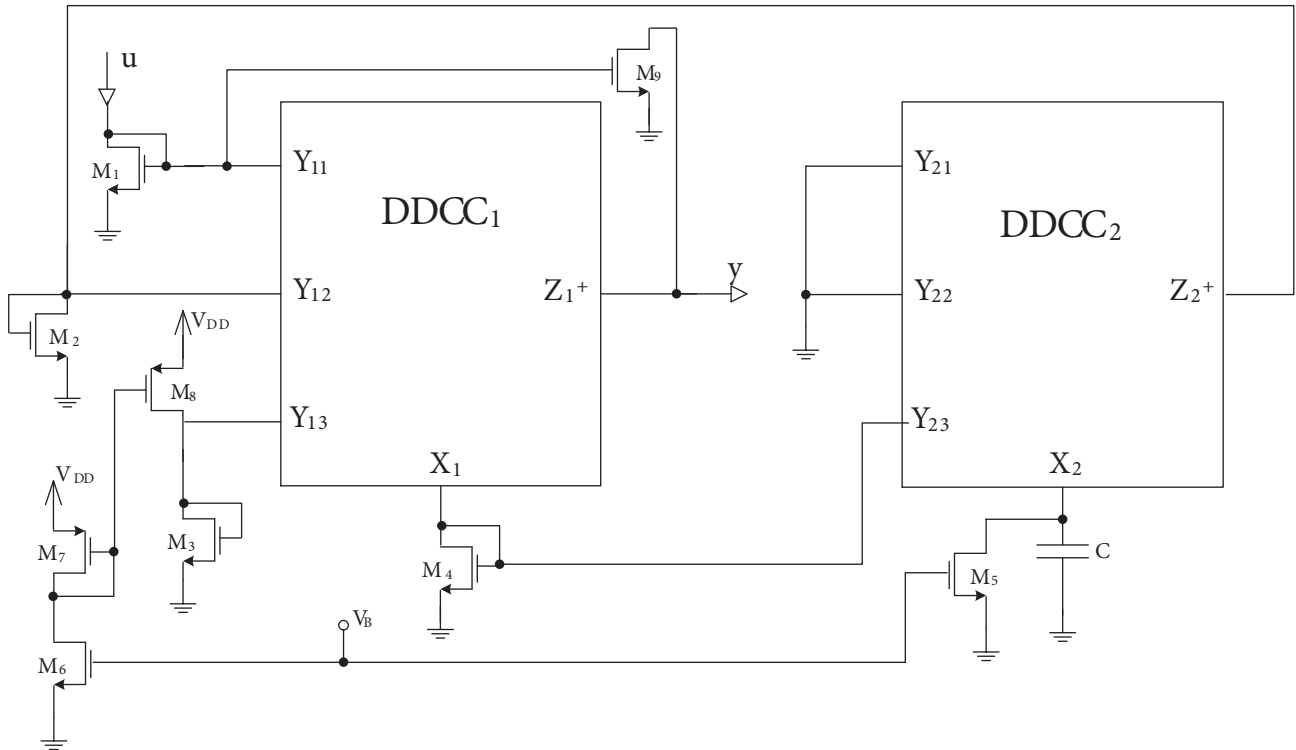
Figure 2. The proposed first-order current-mode AP filter.

2.1. A new high-Q band-pass filter configuration based on the proposed AP filter

The generalized structure of the second-order band-pass (BP) filter configuration is shown in Figure 3. It consists of two cascaded AP filters, one plus-type DDCC, eight external MOSFETs, and three DC current sources. The design procedure of the BP circuit is based on the method presented in [24]. The key aspect of the method is locating two first-order AP filters in a negative feedback loop as given in Figure 3. As emphasized in the previous works [24–26], high-Q BP filter realizations can be obtained by obeying the presented architecture. The output current of the BP filter is given in Eq. (20).

$$y = K_3 u - K_1 K_2 u_f \tag{20}$$

The feedback current (u_f) is scaled with $K_1 K_2$, where K_1 is the gain of the cascaded AP filters (ideally equal to unity), K_2 is equal to I_2/I_1, and K_3 is the scale factor of the input signal. $K_1 K_2$ depicts negative feedback gain. Routine analysis of the circuit yields the following current TF.

$$T(s) = \frac{\frac{K_3}{1+K_1 K_2}(s+\omega_o)^2}{s^2 + \frac{s\omega_o}{(1+K_1 K_2)/2(1-K_1 K_2)} + \omega_o^2} \tag{21}$$

It should be noted that the numerator of the TF contains extra terms when compared with an ideal BP filter. Nevertheless, for high Q values, its gain and phase responses approximate the ideal one near the resonant frequency [24,25].
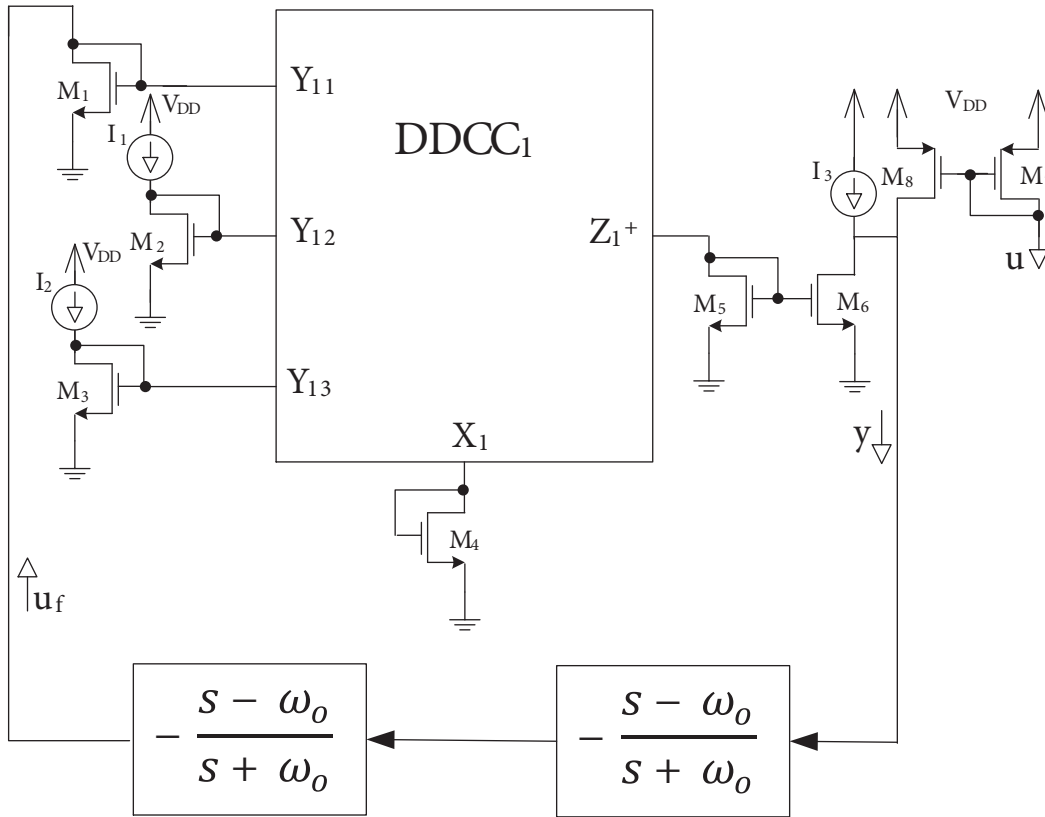
Figure 3. BP filter configuration based on the proposed AP filter.

3. Simulation results

In order to verify the theoretical design of the proposed CM first-order AP filter, a number of simulations including time domain and frequency domain analyses are performed by the PSpice simulation program using $0.13 \ \mu m$ IBM CMOS technology parameters (http://www.mosis.com/cgi-bin/cgiwrap/umosis/swp/params/ibm-013/ t97f_8hp_5lm-params.txt). The CMOS implementation of the DDCC+ is shown in Figure 4 [1]. The aspect ratios of the transistors of the DDCC+ and external MOSFETs are given in Table 1. The power supply voltage of the proposed filter, $V_{DD} = -V_{SS}$, is selected as $1 \ V$. The value of the grounded capacitor of the proposed circuit is chosen as $C = 50 \ pF$ in all simulations. The total power dissipation of the proposed AP filter is found as $2.97 \ mW$ when the control voltage is set to $V_B = 300 \ mV$. Bias current is $I_f = 5 \ \mu A$ in all simulations.

Table 1. Transistor dimensions.

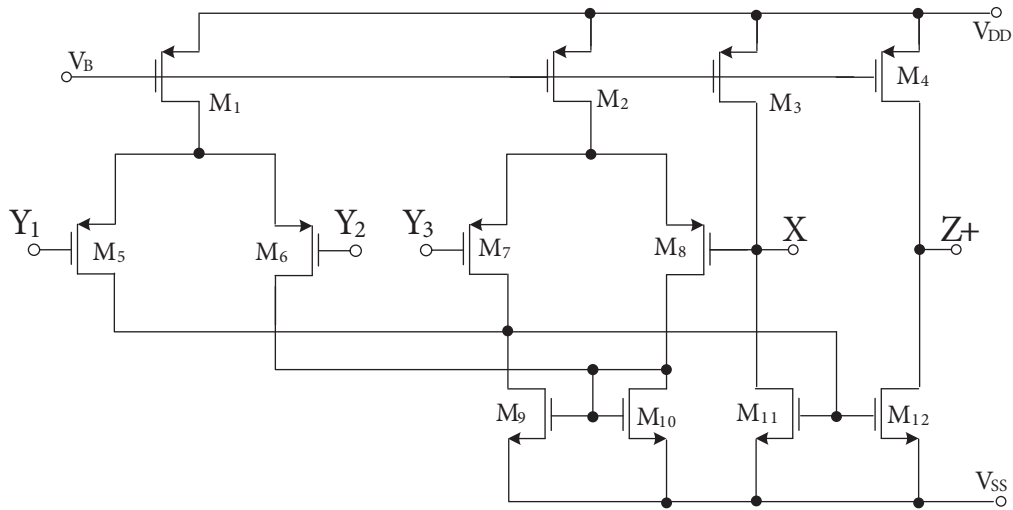|	Transistor	$W(\mu m)/L(\mu m)$
Transistor dimensions of the DDCC+	$M_1 - M_8$	39/1.04
	$M_9 - M_{12}$	13/1.04
Transistor dimensions of the external MOSFETs of AP filter	$M_1 - M_4$	7.8/0.52
	$M_5 - M_7$	3.9/0.52
	$M_8 M_9$	7.02/0.52
Transistor dimensions of the external MOSFETs of high-Q BP filter	$M_1 - M_5$	7.8/0.52
	M_6	7.02/0.52
	M_7	132.6/0.39
	M_8	0.78/0.65

Figure 4. CMOS implementation of the DDCC+ [4].

Both the gain and phase responses of the proposed AP filter approximation are given in Figure 5. The capability of the proposed filter, electronic tunability, is performed as shown in Figure 6. It means that this advantage gives us a wide area of usage without performing modifications in the circuit architecture. The control voltage is swept from $275\,mV$ to $475\,mV$, which changes the pole frequency of the AP filter by more than 1.5 decade (from $492\,kHz$ to $7.5\,MHz$). Moreover, total harmonic distortion (THD) analysis is performed at the resonance frequency of the AP filter for various sinusoidal input peak currents. As seen from Figure 7, the selected operating range remains below the critical distortion limit. Noise analysis is examined as well. Under the mentioned conditions, the output noise value is obtained as $129.7\,pA/\sqrt{Hz}$.
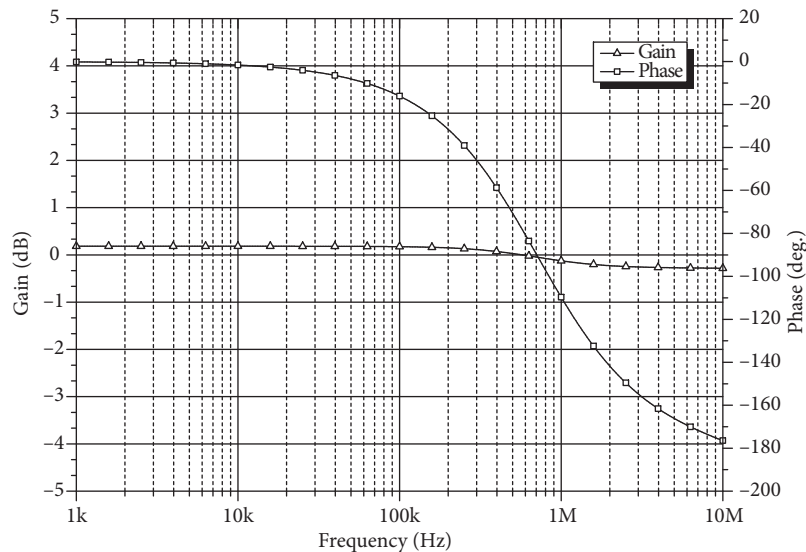

Figure 5. Magnitude and phase response of the AP filter.

In order to observe the effect of tolerance variations of the capacitor, statistical Monte Carlo (MC) analysis is performed when the circuit is set to the same specifications. By arranging the value of the capacitor with

5% Gaussian deviation, the proposed AP filter is simulated. The obtained MC analysis results are presented in Figure 8. Statistical results are offered in Table 2, as well. As is seen, the obtained results are in an acceptable range and the histogram graphic is in accordance with normal (Gaussian) distribution.
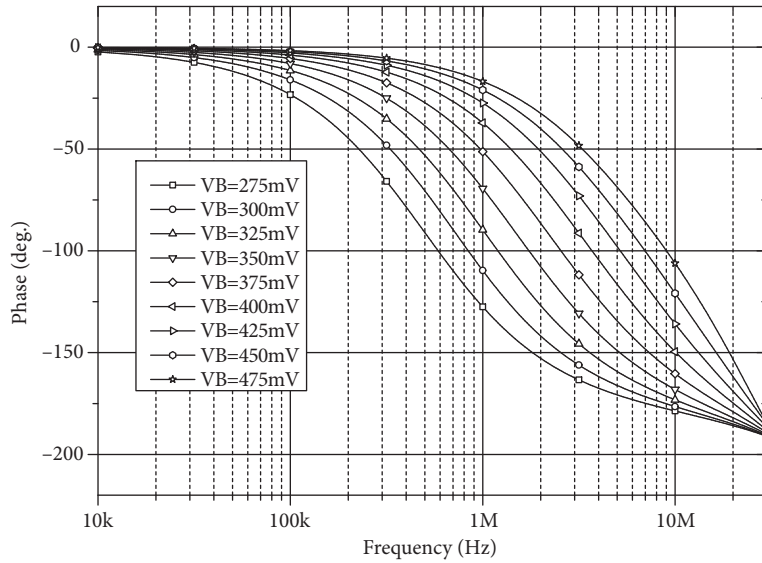

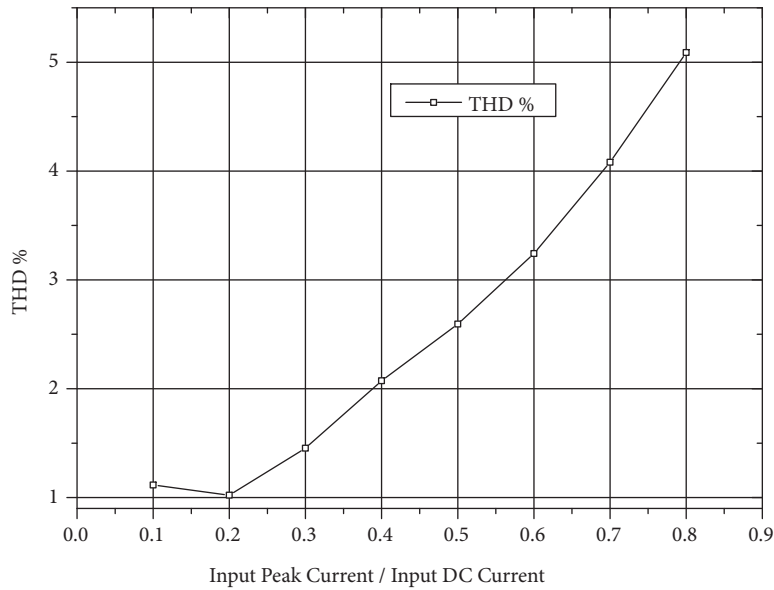**Figure 6.** Tunable phase response of the AP filter.

Figure 7. THD% variations with respect to ratio of applied sinusoidal input current peak value and input DC current.

In Figure 9, gain and phase responses of the proposed high-Q BP filter are given. The control parameters are chosen as about $I_1 = 5\,\mu A$, $I_2 = 7.33\,\mu A$, and $V_B = 335\,mV$, which yields center frequency $f_o = 1.3\,MHz$ and $Q = 75$. It should be noted that the designed high-Q BP filter can be used when a high selectivity frequency response is needed.
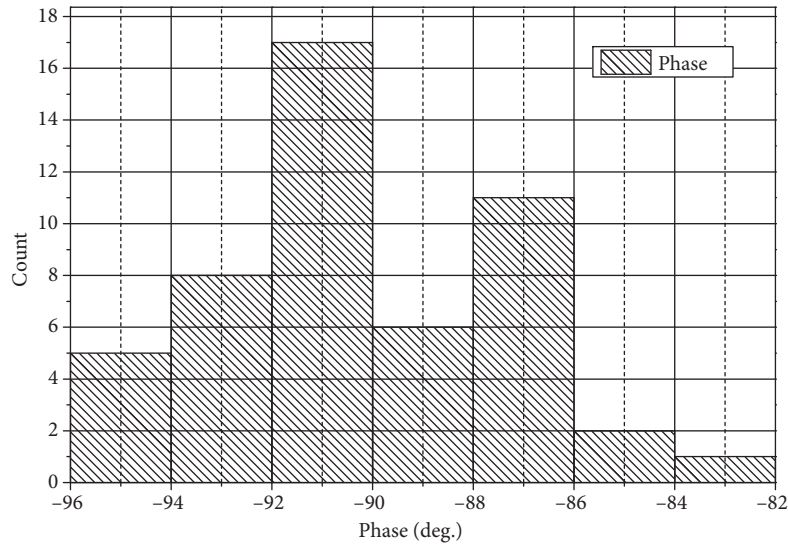
Figure 8. MC analysis results with capacitor (50 pF) providing 5% Gaussian deviation.

Table 2. Statistical results of MC analysis.

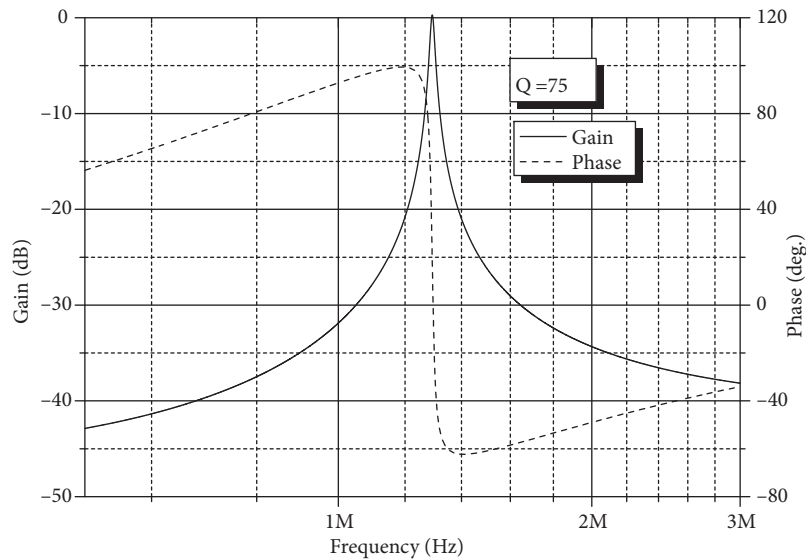| Statistical quantities	Values
Number of samples	50
Mean	$-90.2868°$
Median	$-90.4377°$
Standard deviation	$2.93408°$

Figure 9. Gain and phase responses of the proposed high-Q BP filter given in Figure 3.

4. Conclusion

This paper presents a novel first-order CM active-C AP filter, which employs two DDCC+s, nine external MOSFETs, and a grounded capacitor. Prominent specifications of the proposed filter can be summarized

as follows: signal compressing and expanding after the processing method offering a wide dynamic range (the resulting THD% value is below 5.1% when the peak value of the input signal is equal to $0.8I_f$), very suitable for integrated circuit implementation (proposed circuit consists of only MOSFETs, which use $0.13\,\mu m$ technology, and a grounded capacitor), and electronic tunability without needing any passive component matching constraints (pole frequency is swept from $492\,kHz$ to $7.5\,MHz$ by adjusting only control voltage). The proposed AP filter structure is designed by using an efficient approach, the state space synthesis method. As an interesting application of the proposed AP filter, a BP filter network that can provide high selectivity frequency response is given. In order to show the validity of the proposed structures, several PSpice simulations are carried out. The obtained results included verify the theoretical analysis, as expected.

Acknowledgment

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